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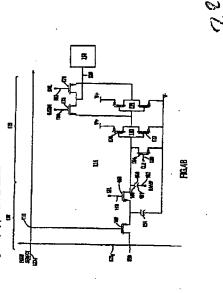
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Analog pixel drive circuit for a display device

(57) An analog drive circuit (114) frait chives a pixel cleatrode (118) in response to an analog sample derived from a vidoo signal. The analog dive circuit comprises a sample celection section (128) and a drive ing a cample lead period. The drive signal generator generates a drive signal and applies the drive signal to the pibal electrode during a display period that follows: signal generator (128). The semple selection section receives and temporarily stores the analog sample dur-

a sequence of a first temporal portion and a second compared portion. The first temporal portion has a time berpousify stored in the sample selection section. The second temporal portion is the temporal compl the first temporal porifon



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Field of the travention

Desoription

play dovices, to enaiog charles for driving the platare demonstric (placies) of vidoo and graphics display desires, and, in perificular, to enaiog direates for driving the place. The invention relates video and graphics disbire elements of a display device based on an electromusical material.

Background of the Invention

8 small crough to be integrated into a halmst or a pair of glasses so that they can be worn by the user. Such wearable display devices would replace or supplement A substitutial need edats for various types of video and graphics display devices with improved performance and lower cost. For example, a need exists for tion larger apperent size, greater privacy, substantially less power consumption and longer battery life than conventional active metric or doubte-coan liquid crystalminiature video and graphics display devices that are used instead of the conventional displays of laptop and davices can provide greater brightness, better resoluthe conventional displays of computers and other devices, in particular, we nable display devices and be other portable computers. Potontially, wearable display bacod displays. Other potential applications of wearable display devices are in personal video mentions, in video games and in virtual reality systems.

displays in low weight and email abo. Of greater prom-tes its a micro display of the type described in United States patent in a \$350.451 of Hambodry et al., the dis-discuse of which is incorporated into this disclosure by been successful in meeting the demands of wearable tive spatial light modulator that uses a tempelectric liquid Ministraced displays based on calinderay lathes or conventional liquid crystal displays have not reference. This type of mions display includes a refleccrystal (FLC) material as its light control element.

stard into a digital bistream suitable for driving the spa-tial fight modulator. The convertar converts the enalog Woo styrel into a time domain binary weighted digital micro display just described is driven by a digital drive The spatial light modulator of the FLC-based by the graphics card of a personal computer, for examthrary weighted digital drive are trinary weighted, so cignal. The conventional analog video signal generaled ple, is find to a converter that converts the analog video the signal suitable for driving the spatial light modulaior. The time durations of the bits of the time domain hat the duration of the most-eignificant bits is 20-1 times of bits representing coch cample of the analog video eignet. For oxumple, il each sample of the analog vidoo eignal is represented by 8 bits, the duration of each most-dignificunitali is 256 times that of each least-eignilthat of the least-significant bits, where n is the number

increases the power domand and exportes of the micro display system. On the other heard, the long time dure-tion of the most expelicant this of the digital drive signal means that the objettle drive signal is actiforter the majorvideo signal. The ewitching speed must be shorter than the duration of the least-significant bit. This requires that the drive circuitry in each phol be capable of high-speed operation, which means that the pixe state several times each frame of the analog teant bit. Driving the pixels digitally by of the frame period. 5

the least-eignificant bits for of the digital office aignals all the pixels of the spatial light modulator, followed by the referred to above typically locate the converter referred to above external of the micro digplay and connect the converter to the micro display by a high-speed digital link. The convertor time multiplexes the cigital drive sigrats for transmission though the digital link as follows: next-least-eignificant bits of the digital orive signals for all the placks, and so on frough the most-exprisional bits of the digital drive signals for all the placks. The digital first must be expected or transmitting all the bits represerting each frame of the component video signal of evilidating at a evindaing speed shorter than the dura-tion of the local eignificant bit, yet remain static for times 10005] Practical embodiments of the micro display within the frame period of the component video signed. The digital first, its driver and receiver must be capable corresponding to the durations of the most-cignificant 설 20

order digital signals generated from the analog video This increases the cost and power requirements of the [0006] In addition, the converter requires a largo, highspeed builler memory to convert the parallel, rester-scan signal to a biforder eignal for each color component.

10007] The digital carial link can be diministed by locating the convertor in the micro display itself, but refocaling the convertor increases the size, weight and completely of the micro display. Moreover, ministurizing the converter to fit it in the micro display can increase What is needed is a ministure display device ics data and that does not suiter from the size, weight, complishly and cost disadvantages of the conventional the cost of the converter. Finally, relocating the conthat can operate in response to a video signal or graph verter chose not recluce its overall cost and complexity. digitally-driven micro display.

(1003) Conventional-sized video and graphics de-plays rely on cathode-ray tubes or full-size liquid crystal daplays. The former are builty, heavy and tragile. The and a limited viewing angle. What is also needed is a ministrum display device that can form the basis of an tomer are also expensive to produce and are very heavy in the larger class required to realize the benefits of high-definition video. The letter are expansive to produce in screen sizes comparable with conventional calhode-ray tubes, and have a limited dynamic range

PAGE 4/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

widea and graphics display that would provide effective alternative to conventional carticolaray tubos and fiquid crystal displays. full-cize : æ

Summary of the Invention

ple keal period. The drive eigenal generator generates a drive signal and applies the drive signal to the pixel elec-trode curton a display period that lobous the sample for driving a pixel electrodic in response to an analog drout comprises a sumple selection socion and a drive elgral generator. The sample selection cocion receives and temporarity ctores the analog cample clump a sam-The drive signal is composed of a The invention provides an analog dive circuit poral porfor. The first temporal portion has a time dura-tion substantially proportional to the analog sample lemporarily stored in the sample selection section. The second temporal portion is the temporal complement of sample derived from a violeo signal. The arraiog drive sequence of a first temperal portion and a second temthe first temporal portion. load parlod.

The sample authout gate opens either during or prior to the display perfod and is disposed between the sample The sanute stonge section may include a cample ctorage element, a sample salection gate, and a sample output gata. The eample selection gate opens ple to the comple storage element and is closed during during the sample load period to actrail the analog sama display period that follows the sample load period. stange element and the chive signal gonerator. (10012) The drive signal generator may include a com-

is corrected. The ramp eignel has a duration equal to is connected, and a second input to which a ramp signal perator that generates the drive signal and that comprises a first input to which the cample selection section

consecutive frames of the video signal. In this caso, the enable drive circuit additionally includes first and sec-The comparator may have a detection sense set by a series cortrol signal having opposite states in in consecutive display periods. The second existing The first switching anangement alternately compacts the cample abrage section to (a) the second input and (b) the first input of (0014) The ramp signed may have a non-linear slope Brangement alternately compects a ramp aignst to (a) the fest input and (b) the second input of the comparator the compressor in consecutive display periods. and switching amangomenta. the display period.

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include an inverter that generates the citive signal, a The offine signal generator may effermatively capacitor and a switch. The capacitor has a first electrade connected to the Irput of the inventor and to the comple selection section, and a second electrode connedted to a ramp signal hawing a chretion organic to the display period. The switch discharges the capacitor to provide gamma correction. prior to the depley poriod.

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The othe signal generator may additionally include a coupling capacitor and an additional switch The coupling capacitor couples the input of the inverter to the sample selection section. The additional swhot lamporarity connects the output of the invester to the input of the invertor prior to the display period. The ewitch is coupled to a reference signal that has a stable oqual to a prodetermined hwenter threshold voltage when the additional switch connects the output of the nverter to the input.

2017] The above-mentioned sequence of the first be a first sequence of the first temporal portion and the second temporal portion and may have a duration equal to one half of the display period, and the drive signal generator may generate the drive signal in a first electrical state during the first lamporal portion and in a secand temporal portion may be in any order in the second amparal partion and the second temporal portion may ond efectrical state during the second temporal portion. in this case, the dilive signal generator may generate the drive signal additionally composed of a second sequence of the first temporal portion, in which the drive signal is in the second electrical state, and the second temporal portion, in which the othe signal is in the first electrical state. The first temporal portion and the secenquence. The second sequence rectores the DC balence of the pixel. 8

a pulse hanking a second potently, apposite the first pola-ity, at the beginning of the second portion. To generate this drive signal, the drive signal generator may include When the analog drive orous is for driving an polarity at the beginning of the first tamporal portion and eloctro-capical material having a biotable characteritis, the drive signal may be composed of putse having a first En B.C.-coupled output. 8 Ħ

Brief Description of the Drawings

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Agure 1 shows the structure of a display device that incorporates the enalog drive circuit according to

Figures SA-3D illustrate how analog samples are derived from the wideo signal and distributed to the make the chart of each phal in the phal array of the aparial light modulator shown in Figures 2A-2D. the tree fames of the video signal shown in Fig-ures 3A-3C stored in the sample education section of the analog drive circuit of an exemplary pixel of Figures 2A-2D show details of the speakel light mod-Figure 3E shows the analog samples derived from ulator of the display device shown in Figure 1. he pixel array.

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Figure 9F shows the drive signals generated by the pica shown in Figure 3.E. Rgure 4.A is a block diagram showing the pixal malog drive drout in response to the amilog sam-

PAGE 5/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

device that incorporates a first enfortement of the Figure 48 is a coherrentic chagram of the livel cuit of e first embodiment of a monodirome display array and the cample derivation and distribution ciranalog drive circuit according to the invention.

Figures SA-6D are waveform degrams illustrating the uperation of the embodiment of the display

embodiment of the enalog drive circuit according to

he invention.

nation and distribution clausi shown in Figure 4A Figures 7A-7G are waveform diagrams illustrating Figures 64-6R are waveform diagrams Bustneting the operation of the embodiment of the sample derdavice shown in Figure 4A.

2

that inhibitizes variations in the effective offset of Figure 8 is a cohemetic diagram of a variation on the first embodiment of the analog drive circuit according to the invention that incorporates circuitry chout shown in Figure 48.

Figures 6A-60 are waveform diagrams flustrating the drive signal generator.

Figure 10A is a block diagram showing the pixel the operation of the offset minimizing circuity of the auit of a second embodiment of a monodrome dis-play device that incorporates a coord embodiment of the analog drive circuit according to the Invenentey and the sample derivation and distribution caembodiment shown in Figure 8.

Figure 108 is a schematic diagram of the second embodiment of the enalog drive circuit according to

ing the operation of the entocliments of the display donce, the sample derivation and distribution drautt and the analog office circuit shown in Figures 10A Figures 11A-11O are waveform diagrams illustralthe Invention

Figure 12 is a block dagram of en exemple of a switched-sense comparator stabble for use in the embodinaris of the analog dave drauk shown in Figures 108, 15C and 16B.

a variation of the second embodiment of the mone-Righte 18 is a block diagram showing the pixel array and the sample derivation and distribution circuit of Jenheison and distribution circuit shown in Figure ing the operation of the embodiment of the sample Figures 14A-14F are waveform diagrams Bustratdrome display device.

¥

Figure 15A is a block diagram showing the pixel array and the panellel-load sample derivation and distribution circuit of a first embodiment of a color display device that incorporates a third embodiment of the enalog drive circuit according to the invenFigure 15B is a schomatic degram of the third embodiment of the snalog drive circuit according to

Figure 15C is a cohematic diagram of a fourth embodement of the enables drive circuit according to the Invention for displaying a color video signal. Figure 16 is a block diagram drowing the pixel array and the sarial-load sample derivation and distribu-tion circuit of a second embodiment of a color disembodiment of the analog drive circuit according to the invention for displaying a color video signal play device that incorporates the the invention.

Datalled Description of the Invention

device 10 according to the invention that includes the reflective spetial light modulator 100. Other principal components of the display device are the light cource Figure 1 shows the structure of the display 15, the polarizer 17, the beam splitter 19, the analyzer 21 and the eyepieco 28.

2

The operation of the embodiment of the analog drive

driver 67 that drives the LEDs 69-71. The LEDs are of (4021) The fight source 15 is composed of the LED different colors and are independently driven in a color ance to Figures 15A and 16. Fower or more LEDs, or display device, as will be described below with referother light emitting devices whose output can be rapidly modulated may atternatively be used as the light source As a turther ofternative, a white light source and a ight modulator may be used. The light modulator mod-8 ĸ 8

ulates the amplitude of the light autout by the light saures and, in a entor design Goldee, autilitionally modulates the color of the light output.

policy | The light source 15 generates light that possess immugh the policative 17. The been spirite 19 relicats a the layer St of electro-optical material (the electro-opti-cal layer), to be described below, the direction of polari-zation of the reflected light is either unchanged or is rotated through 90°. The reflected light passes to the haction of the polarized light from the polarizer towards the spetial fight enodutator 100. The reflective electrode 85 located on the surface of the substrate 89 of the spetial light machdator reflacts a teaction of the broldoni potentized fight. Depending on the electric field across ucars eye E through the beam splitter 19, the analyzer \$

(0023) The eyepiece 23 focuses the light reflected by the reflective electrods 85 at the user's eye E. The eyeplece is shown as a single convex lars in Figure 1. A more complex aptical enengement may be used to form a lorr-aberration image of the desired apparent size at 21 and the eyepiece 23.

The direction of polarization of the analyzer 21 is aligned parallel to the direction of polarization of the polarizer 17 so that light whose direction of polarization has not been rotated by the spatial light modulator will pass through the analyzar to the user's eye E, and light trough 90° by the epatial light modulator will not pass fricugh the analyzer. Thus, the analyzer prevents light direction of polarization has 8

PAGE 6/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

whose direction of potentration has been notable by the apetrial by the modulator from resolving the user's eya. Consequently, the spatial light modulator is not standard will appeal light or dark to the user depending on the applied electric that When the spatial light modulator appears Right. It was be set to be in the ONF state. The direction of potential was able to be in the ONF state. The direction of potential on the area year of the the Conference of the standard or the control of the area of the potential. This case, the spatial light modulator operated in the opposite corne to the tips (described. The entities a positive picture to be obstituted by its untentities.)

(OCCS) The optical arrangement shown in Figure 1 may also form the basis of a full-time video or graphics display. The inventors have demonstrated such a full-class color display device with a nominal deagonal dimension of 450 mm. This display device was made by increasing the intensity of the light source 15 and by inspecting the eyesteece 23 with magnifying optica that form an image of the reflective electrode 55 on a sailtable or man image of the reflective electrode sequencially flurmated by the of the first prinary colors, or portificient primary colors, each flurithzed by light of efficient primary colors, can be used in a full-size color.

form an image of the reflective electrode \$5 on a sailsble account A single scralal light modulator sequentially
illuminated by light of the tree primary colons, on paralilluminated by light of the tree primary colons, on paralilluminated by light of the primary colons, on paraldiffers trimmy order, can be used in a fall-size order
display device.

IQUED! Figure 1 autificiantly shows some deside of the
special light modulator 100. The special light modulator is
composed of the olectro-optical lique 31 cambridated
for electrode 35. The electrode 38 is transparent and its
singuished on this surface of the transparent cover 37.
The electrode 35 is forced on the surface of the semianticiping at heavents so.

between the common electricia 33 and it a reflective describe 35. In a electrode 38 is transparent and is deposed on the surface of the transparent and is control of the surface of the service of the service or the depose or the depose or an explicit electrol or optical property that objects on an explicit electrol or optical property that objects on an explicit electrol or optical property or optical property or an explicit electrol or the depose or an explicit including on the electro-capical layer deposed on the deviction of the deviction of the deviction of an electricity of the deviction or an electrol or the deviction of potentiation may deposed on the strength of the deviction of deviction or the electron of the deviction of the deviction

flett quplicit to the layer.

[1022] Some electro-optical materials have a bistration draisedreffel, in such materials, the optical property of the materials is set by applying a bord-clumforn electrical purses. The material will leagh the optical property set by the deforting layer will the material is reset by applying a ford clumforn optical pulse in the optical property set by the decirical pulses will he material is reset by applying a ford clumforn optical pulse in the optical applying a ford clumforn optical pulse in the optical behavior provided behave one officiency companied. This provides i they are they are forced behave need the provided. This provides in farger furthroad efficiency companied with elec-

(0029) In the preferred enhancement, the electro-optical material is a tencelearic liquid orystal material. The direction of the electric float applied between the transparent electrode St and the reflocine observed in the transparent electrode St and the reflocine observed impairing on the ferroelectric material sanderind impairing on the ferroelectric material sanderind between the electrodes is rested or not. In other entod ments, a conventional nematicity, or not in the section optical material, in this case, the strongly of the electro-optical material, in this case, the strongly of the electro-optical material, in this case, the strongly of the electro-optical material, in this case, the distength of the electric fleat between the electrodes determines whether the direction of potalization is notated or not.

(8030) To enable the display derive 10 to display on image instead of mently cartholling the passage of light to the light scarce 15 to the usest's eye. E, the ration-the electrode 35 is divided into a two-dimensional array of pixel dectanded, enemplay criss of which see shown at 118, in addition, an enablog drive decall according to the invention (114 in plays 24) that directly the plays a bordown of the invention (114 in the substrate 39 turder each play an electrode. The arrange drive directly the plays each play electrode and the portions of the doctino-quities layer 31 and the common electrode 33 evertaying the plast electrode and the portions of the doctino-quities layer 31 and the common electrode as seemblely one of which is

se shown at 112.

(DOST) When the dectro-optical layer 31 is composed of a ferrobestic metrics, the direction of the dectrication of a ferrobestic metrics, the direction of the dectrication between seath pixel dectrods, such as the pixel dectrods 118, and the comman electrods 30 determines whether the dection of polatication of the layer reflected by the pixel dectrode is related through 50° or not, and thus whether the corresponding pixel. Such as the pixel into a pixel into order to the user when the pixel appears bright or clark to the user when the pixel appears that it one such that it of No state, and when the pixel appears that, the pixel will be said.

source 15 and reflected by the pixel either passes frough the analyzer 21 to the user's eye E or does not a grey scale, the apparant brightness of each pixel is varied by temporally modulating the light that reaches the user's eye. The light is modulated by choosing a The optical characteristics of the phoets of the spatial light modulator 100 are binary. Light from the fight pess through the analyzer to the user's aya. To produce besic time period that will be called the illumination perhod of the spattal light modulator. The spatfal light modulator is illuminated through the Humination period and each plosal is set to its ON state for a first temporal portion of the lituralization period, and to its OFF state for a second temporal portion. The second temporal portion constitutes the remainder of the illumination period, and is thus complamentary to the first temporal portion. Alternethydy, the OFF state may precede the ON state. The fraction of the liumination period constituted by the first temporal portion, during which the pixel is in its ON state, deformines the apparent brightness of

To maximize the service life of the spatial light

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widhed between the transparont cover 37 and the semiconductor substates 39. The transparont cover, lucent common effectinde 89, which may be a layer of indum the code (ITO), for example, is located on the 20. Referring first to Figuros 2A and 28, the light madulator is composed of the electro-optical layer 31 sandwhich may be a thin glass plate, for example, is suparated from the substrate by the spacers 108. The transheide surace of the transparent cover, facing the subdescribed in more detail with reference to Figures 2A 5 modulator, the DC balance of each pixel must be main-Umo-integral of the electric field conventional (non-bisseate) ferroelectric material during the first temporal portion is rarely equal and opposite to that applied during the second temporal porflon, additional measures must be taken to restone

800 2 to zono. This is accomplished in practice by driving the is roctored by driving the pixel so that the electric field applied to the fermelectric material of the pixel everages ing the illumination period is followed by a second the DC betance of the pixel. The DC betance of the pixel pixel electrode so that the first sequence of the first temposal partion and the second temporal portion constitut-

sequence of the first temporal portion and the second temporal portion, the second sequence constituting a Yors of the balance period, the etals of the drive signal is the same as fact during the second and first temporal periods, respectively, of the Burninston period. To prevert the batance period tollowing each Rummation solation period, in the first and second temporal porperiod from causing the display device 10 to display a unitern, grey image, the light generated by the light source 15 to modulated so that the spatial light modulafor 100 is only illuminated cluring each illumination period and its not alternitizated during the following teat-

light modulater. The display period of a monodrame display may correspond to the frame period or the pic-The Munication period and the balance period collectively constitute the display period of the spatial ture ported of the video signel, for example.

As noted above, the other signal required to drive a historia electro-optical material during the Burniquently, no balance period need be provided, and the charafon of the flurnination period can be extended from netion period can be inherently DC balanced. Conseabout 50% of the display time to about 100% of the dis-9

light source 15 fluminates the spattal light modulator with light of a different color during the flumination perbod of each display period. Each pixel is ent to its ON state for a fraction of each of the three flumination perforts and to its OFF state for the remainder of the litumination. The principles just described may be expended to onable the spailal light modalator to generale a color by the color components of a color video signal, and image. In this case, the spatial light modulator is driven three display periods are defined for each frame of the color video signal, ono for each color component. The each of the three determines the apparent enturation and has of the pixel. to one-third of the frame period of the color video for example. Making the display period the same Burnination periods in which the pixel is in its ON state The display periods of a color display may each correnation period. The fraction of good

The spatial light modulator 100 will now be

of the substates 39. The examplery pixel is shown at 112. The drawings froughout this disclosure drow pixel arrays with only four pixels in each dimension to simplify. would be composed of, for example, $640\times480,\,800\times600$ pixels, 1280×1024 pixels, 2044×1125 pixels, or An array 102 of pizets is located on the surface the drawings. In a practical embodiment, the pixel emay some other acceptable two-dimensional arrangement of

For each pixel in the plxel array 102, an arratog ventional commandurant processing on and under the surface of the substrate 39. The analog drive cloud of the eigenplary pixel 112 is shown at 114. The analog fortal layers of conductors (not shown). The surface of the sthatrate, and the above-mentioned layers of conductors, are covered by the insulating layer 116. The reflective pixel electrode 118 of the pixel 112 is located othe circuit is composed of transistors, capacitors and other, aircuit elements (not shown) interconnected by one or more layers of conductors (not shown). The arelog drive chauts of the polals constituting the post amay log offive circuit. The pixel efectode is connected to the drive circuit according to the invention is formed by con-102 ere connected to one another and to pack through which external electrical connections are made by addon the surtace of the insulating layer overlaying the ansoutput of the ensiting office circuit 114 by the conductor 120 which passes through an aperture formed in the (850g) 8 S a

(0040) In the pixel 112, the anatog drive circuit 114 genericates a drive signal that is explice to the pixel electrode 118. The drive signal applied to the electrode has a 1 state and a 0 state. The 1 state may be a high volve. the electro-quical layer 31 overlaying the posel elao-incde rotates the direction of potentization of light falling age state, and the 0 state may be a low voltage state, for example. The state of the drive signal applied to the pivel blactrode determines whather or not the portion of cuit sats the apparent brightness of the pixel by applying on the pluet, as described above. The analog drive cirthe drive signal to the pixel electrode in response to an snatog sample derived from a video signal. During each above-described liturihation period the drive signal starts in one state, corresponding to the CN state of the pixel, for example, and remains there for the first temporal portion. Before the end of the illumination period, the thire signs switches to the other state and remains Insufating layer.

thoro for the assord temporal portion. The fraction of the illumentant part of without the pixel is in its ON state determines the apparent brightness of the place. When the wides opiral is a color wides object, the surdog dhine droit is east the apparent extunction and have of the pixel by applying drive signals than the pixel ON to Residons of these consecutive illumination periods that deport on the fitnes color components of the color wides shown.

(1004) The victoe signed may be a conventional analog vidoo eignal such as is generated by a conventional computer graphics sets, about what or staken's necessary to produce the described below, a conventional making vidoo signal may be computer graphics disso such as is led to a computer graphic disso such as is led to a computer graphic additional and graphics disso such as is led to a computer graphic addition or generated by a digital vidoo or television receiver. In this case, conventional activities droutly y (for shown) is provided to convert the digital graphics didta but an analog video signal, or to durine directly from the digital graphics did graphics did a mando when signal and mando when signal or to durine directly from the digital graphics did the analog expenses.

distributed to the entroig drive drouble of the pitchel.

[10042] Fugure 2A strows the pixels entranged in the twodimensional pixel entry It2 on the surface of in the twostrate St. The sample defineds and distribution drouble.

104 is data farmed in the subchara 83. This drouble drouble

thickes analog samples defined from the victor aginal

recorded wife the victor pixel 106 to the pixel amy and

plenetates. The pixel entry Signals are distributed from

the sample definedies and distribution crount to the pixel

de by butsess, representation correct of which are schown

schomathalp at 181 and 183.

required by the posel array. Signals are distributed from as the sample derhaden and distribution carbail to the pictors of by busses, representatine ones of which are aboun schomadcally at 181 and 183.

[0043] Figure 2C is cathematic representation of the clouds arrayoners of the special light modifator solution. The area carbain and the special light modifator solution. The area carbain and derives a stroom of analog samples from the video signal. The analog samples from the video signal. The analog samples from the video signal. The analog samples are distributed to the pixels constituting the pixel array 102 by the sample destruction cross 124. Earth or pixel receives at least one sample of each frame of the video signal. The broniform in the frame of the video signal. The broniform in the frame of the video signal where the sample is donived commonstrate to the frame simple array as a threatent of the Figures 3A-810.

10044) Figures 3A-8C respectively show examples of three constroative traines of the video signal received with the video signal received with the video input 106. Each frame is shown divided into true sequentially the faure of the place array 102. Each line is shown divided into two earths, corresponding to the four pixels in each raw of the place array. The arrading sample generated by the arrading sample generated by the arrading samples derived in response to each segment of the video signal is inclinated by a short incircual line. For exemple, the arradio samples derived from the segments 123, 123, 2 and 123, list, the second segment of the second line of each frame, are indicated by the horizontal lines 125, 125, and 125, respectively.

pi045] The row and column numbers of the pbess in the pixel array 102 to which the sample distribution of-outh 124 distributes the analog semples are indicated in Figure 30. For example, the secretion of the pixel error, and so receives the enalog samples 1254, 125₂ and 125₃ respectively derived from the segments 1254, 125₂ and 125₃ respectively derived from the segments 1254, 125₃ and 1253, 1254, and 1253, and

(9046) Figure 2D is a schemation parasoniation of the clockfull arrangement of the pixel 112 in the two dimensional plants array (12. The manning plass have the same electrical arrangement. The pixel is composed is of the suralog drive sicuril 114, the cutual of which is connected to the electrode 118 by the conductor 120. The arrange drive circuit is composed of the sample selectron cockion 125, and the other delay generator 122. The sample selectron social near the cample significant of the trange of estimation denial 124 (Figure 2C). During each trane of the video signit, the sample selectron section receives an arrange sample derived from the video signit will the sample input and lattrocarly stores the sample wird free sample input and lattrocarly stores the sample of elevation the trange of the video signities derived from the sample generator 128. Figure 3E efform the arrange samples defined from the tree frames of the video signities from the first 112. [D041] The drive cignal generator 128 roodwoc coch

account massage became section for pour 112.
[DM1] The drive doptal generator 128 road-oc each serial grample stated in the sample selection section 125 during the picture ported of the provious frame and in response to the sample generates a drive signal and applies are drive agraal to the electrode 118. The drive signal serial generates the drive agraal with a period conseponding to the above-described display ported. Figure 3F strows an example of the drive agraal openedate by the analog drive draft 114 in response to the arrange surplose shown in Figure 3E. Each of the display ported of the analog drive draft 114 in response to the arrange surplose shown in Figure 3E. Each of the display perbots of the drive agraal is composed of an illumination of the faste for a distal temporal ported at 124 in the drive agraal generator at each illumination of the first lampcal ported of the corresponding of analogs sample. This can be seen by comparing the during are of the first lampcal ported at 174 of liamination periods shown in Figure 3E with the corresponding viding electes shown in Figure SE.

\$0.43] The drive signal to generated so thet it remains of in the 0 state for the second temporal portion 2.1P consisting the remainder of the fluorisation period, and elso for the first temporal portion 1TP of the belance period. The first temporal portion of the belance period. The first temporal portion of the second period or which the drive agreat was that it state for the signal dennyes or the 1st temporal portion of the state for the signal dennyes or the 1state for the belance period or the belance period. The correlating the remainder of the belance period. The duration of the

portion of the drive eignal is different in voltage lend of the respective cample, in each following balance period, the drive signed is in the 1 state for the second temporal portion, and is therefore in the 1 state each of the three atunination periods, depending on the by a firme that is complementary to the charation of the 1 stato in the Alumination period.

10049] In the example shown in Figure 2F, the display period of cook frame begins immediately after the end of the display period of the previous trame. In some below with reference to Figures 4A and 4B, the chive waveform is generated intomittently, and a period in embodiments, such as the embodiment to be described

eventule, an arraby drive crout capable of generating the waveforms just described can be adequed to drive a blistable electroperioral marieria by capablathery or a.c. accuping the output of the crook to the pixel electrode. [QGS1] Figures 4.4 end 40 show a first presization procinent of the circuity of the speakel light modulator. which the drive signal is generated in a neutral state to bringosed batwoen consociative display periods. (10050) The wendlorms just described are those required to drive a electro-optical material that lands a tistable dranacteristics. However, it will be appearent to a person of ordinary stidl in the art that circuits, such as frose to be described below, for generating such waveand distributes the samples to the individual pixels. Fig-ure 48 shows the snatog drive circuit of one of the pixels in detail and will be described below. In this embodiforms can easily be adapted to generate the waveforms required to drive a bisnebbe electro-optical material. For 100 in more detail. In particular, Figure 4A shows in more defail the sample derivation and distribution of roat 104 that derives arcabg samples from the video signal ment, cample selection circuits that perform the row-wice distribution function of the sample distribution chcircuits of the pixels. The analog compling circuit 122 of the pixel array 102, and the sample section arrait in cuil 124 shown in Figure 2C reside in the analog othe generales a stream of analog samples for each column each plust performs the row-wise eelection from the sample stream (2002)

highly-simplified 4 x 4 amay of pixels to simplify the to a morrochrome display dovice based on a drawing and the explanation. A variation that provides a color display device will be described below with refer-This embodiment will be described with reference to Figure 15A and 15B.

MICHO SIGNAL Y viz the wideo imput 106. As will be analog othe count eddisonally has a ramp input and additional inputs for various firming and control signals (not shown in Figure 4A). Each analog other chould delivers a other signal to the decardes first overlays it. The analog sampling circuit 122 receives the described in more detail below, the analog office circuit of each pixel in the pixel array 102 has a semple input and a row select liquit. For example, the pixel 112 has the comple input 150 and the new select input 110. The

log camples received by each column of pixels are derived depends on the location of the column in the pixel array, as described above. An analog cample of amay are connected to a column bus that is in turn connected to a respective output of the analog sampling drount 192. For exempte, the sample inputs of the phase In the second column, where the exemplary pixel 112 is located are connected to the column bus 131,2. The location in each line of the video signal whence the aneovery line of the video signal is fod to the sample liqual of each analog drive circuit

(19064) The row select inputs of all the pixels in each row of the pixel energy 102 are connocted to a row soloral but that is driven by a corresponding output of the row plusis in the second row, where the eventylary plus 112 is located, are connected to the row select bus 133₂. An video signal, the row selector sets the row select bus 1331, connected to the first row of pizels to the 1 state, estator 134. For example, the row select inputs of the at its sample input only when its row select input is the 1 state, for example. The row selector sequentially sets Adde signal. During the first line of each frame of the first column. The column bus of each octum leads the arelog samples to all the pixels in the octumn, but the analog samples are only eccepted by the pixels in the enatog drive circuit can accept a analog sample present the row select busses to the 1 state at the line rate of the and sels the remaining row select busses to the Distata. The sampling circuit 182 sequentially feeds analog samples of the first line of the video signal to the column busses in order, starting with the columntus 181, of the ×

pixels to the 1 state. When the sampling croul 132 sequentially feeds analog samples of the second line of the row select bus 188₂ connected to the second row of (1005-5) At the end of the first fine of the video signal, row selector 134 sets the row select bus 133, connected to the first row of poods to the 0 state, end sets the video signel to the column busses, the analog samof pixels. This process is repeated with the row safector sequentially setting the remaining row select busses 1883 and 1884 to the 1 state until each pixel in (0056) The part of the englog sempling circuit 122 that ples are only excepted by the ploats in the second row the pixel erray 102 has accorded a different analog sample derived from the frame of the video signal. 3

defives analog samples from the video signal and the sample escripte distribution obcuit 124 that feeds the analog surrictes to the sample input of the analog drive circuit of each of the places in the pixel array 102 will now be The video signal is fed from the video fraul 106 to the buffer amplitier 196. In addition to bufferfing the drange the dynamic range and DC level of the video signal, the buffer amplifier unay exclinionally dynal to meet the dynamic range and DC level requirements of the analog office drouks of the light modulato 200 e G

13

100. The video signal Y_G output by the buller amplifier ts ed to the camping drouit 192. The builder emplifier may attentatively be omitted.

sample and hold (SH) circuit for each column of the omitted. Each of the GAI chourts has a signal input S, a colum edector 140. For example, the control input of the SM circuit 1884 is comedad via the control line 1894, to the output 1411, of the column selector. The The sampling circuit 132 is composed of one other then the SM circuits 138, and 138, have been is connected to receive the video algms! Yo output by example, the output of the SM circuit 138, is commeded to the column bus 131; commeded to sample impulse of the analog of the circuits of all the pixals in the first colphoel array 102. To company the chrowing, the SVH coronies nected via a control line to a corresponding output of the control imput Cand a sample output O. The signal imput the buffer emplifier 136. The control hipset C is concample curput O of each SM circuit is connected to the column bus of the respective column of pixals. For

(10039) The column selector 140 receives the chark eigened PDCL from the clock genomer 142. The chark eighted PDCL includes a phash-ata chock signal and the horizontal sync algual extracted or otherwise derived described in more detail below. The column selector is from the video signal. The clock generator will be are connected via control knee in column order to the control inputs of the sampling circuit 192. For example, the output 141, of the first stage of the shift register is connected via the control line 189, to the control input of the SAH circuit 138, of the sampling circuit.

erray 102. The outputs of the stages of the shift register line 139, is set to its I statu, and the cutouts of all the other stages are set to that 0 states. Then, the chock signal PUKEI progressively shifts the 1 state atong the corrobosed of a shift register (not shown) having stages equal in number to the number of columns in the pixel (10060) The treating edge of the horizontal sync signal or the horizontal blanking signal recess the shift register register changes from 1 to Q. The sample cutput of the SM circuit 1984 is set to a value that represents the lavel of the video signal cluring the proceeding pixel constituting the column selector 140 so that the first stags, whose output 141, is connected to the control set to a value that represents the loval of the video signary corrected to the signal input S of the S/H dreuth. For example, as the output 141, of the first stage of the shift shill register at the pixal rate. As the output of each ple output O of the SM dirait controlled by the stage is stage of the shift register changes from 1 to 0, the samperiod. The sample curput of the SAH drouit may be set signal at the time the control Input to the SAH chould

video eignal during the fine that the control input is in its 1 state, depending on the sampling characteristics of The structure of the row selector 134 is similar to that of the column selector 140. The number of tor is equal to the number of rows in the pixel array 102. The row selector receives the chock signal LINE from the dock generator 142. The clock signel LINE includes a Instructe clock signal, and the vertical sync signal edracted from the video signal. The row solution is stages in the shift register that constitutes the row salac reset by the trailing edge of the vertical sync signal and the row selector exocossivoly activates the rows of pixis clocked by the Uno-reta clock signal. Consequently, els at the line rate of the video signal.

(2002) The clock generator 142 receives the video signal from the video trout 105 and generates the vertous the art and so the clock generator 142 will not be described in detail here. The clock generator leads the control signals SEL, CLE, ILLUM and BAL via the bus 112 for distribution to the enalog drive circuits in the pling circuit 122, the analog drive circuits of the spetial light modulator 100, the ramp generator 144 and the LED driver 67. Suitable clock generators are known in clock and control signeds required by the analog samobsel ermay 102. R

tor derives synt signels from such alternative indicated the start of the transe and lines of the video signal as * horizontal sync signals from the video signal. If the (8063) As part of its chock and control signal generafor, the clock generator 142 extracts the vertical and Ivideo eignal factes such sync signals, the clock generaare included in the video signal or are otherwise availa-

(1064) The LED driver 67 receives a control signal from the dock garestator 142 and drives the LEDs 69-71 (Pigure 1) in response to the control signal to cause the LEDs to Runinate the spatial light modulator 100. The traing relationship between the drive eignal applied to . The LEDs and the control algorats applied to the spatial light modulator will be described below. 셤

(0065) For each frame of the video signel, the ramp For exemple, the ramp generator generates the first ramp signal in response to the trailing edge of the vertical sync pulse, and generales the second ramp signal in the ramp signals are depicted as having linear slopes in and effective garrms correction. Garrms correction is required to correct for the non-linear perception of the genorator 144 generates two successive ramp algnats, response to the end of the first ramp signal. Although ably non-linear sizoe a non-finear slope provides simple cach having a duration equal to the illumination period The drawings, the slopes of the ramp signals are profer apparent brightness of the pixel by the human eye.

[0066] A existable non-linear ramp signal may be gen-ermad using a mamory. Values that define the land of the ramp signal at times corresponding to each cycle of a clock aignal, such as a clock signal obtained by divid

changes state, or the peak, or mean, or RMS texal of the video cignal during the period in which the control input is in its 1 state. Attematively, the cample output of the I circuit may be set to some other level related to the

percenting a suitable non-linear ramp signal by digital or Ing the pixel clock signal, are stored in the memory. The memory is then clocked with the clock signal, and the verted to an analog rump signal. Other techniques for leads the ramp signals via the bus 113 to the pixel array auccessive volues read out from the memory are conmalog means are known in the art. The ramp generator 102 for distribution to the analog drive choults of the plaels in the errey.

1067] The ranp agrais generated by the ramp generator 144 eve shown in Figure 70 and 11J below as beginning in a low clate and increasing towards a high state. However, this is not oritical. The name aignets may Moreover, the ramp signal may begin in the low state begin in a high state and decrease towards a low state. Bion period and may then decrease towards the low and increase towards the high state during the Illuminastato in the following belance period, or vice versa.

A first embodiment of the enalog drive areuit econding to the invention of each of the pixels of the pixel state of the pixel army 102 is shown in Figure 4B. The analog drive second row of the pixel array. The enalog drive circuits of the other pixels of the pixel erray are identical, but plary analog drive circuit 114 of the exemplary pixel 112 circuits will be described with reference to the exem shown in Figure 4A. This pixel is the second pixel of the each is comedad to a different combination of column bus and row selector bus.

During each frame of the video signal, the ana-

log drive circuit 114 receives on analog sample derived from the video signal, generales a drive signal in responso to the analog sample and applies the drive This embodiment of the analog of the circuit 114 signal to the pixel electrode 118.

the column bus 191₂ and stores the analog sample. The drive signal generator generators the drive signal and applies the drive signal and applies the drive cignal to the pixel electrode 118. can be regarded as being composed of the sample sarrple for the pixel from among the analog camples on described. The sample selection vection selects and be displayed by the pixel 112 from the analog samples solociton section 126 and the chine signal generator 128. The sample selection section selects the analog The sumple selection section 128 will may be stores the analog samples of the video signal that are to placed on the column bus 131₂ by the sempling circuit 132. The sample selection contion also leads the stored

The sample input 150 of the analog office circuit 114 is connected to the column bus 1312. Also connected to the sample input is the drain of the semple The gate of the sample select ransistor is connected via the row select input 110 to the raw select bus 133, connected to all the pixels electrods of the semple storage capacitor is connected of the comple select translator is connected to one elecrode of the sample storage capacitor 154. The other enakog samples to the drive signal generator 128. select transistor 152,

nected to the sample output control signal SEL gonerated by the choic generator 142 and distributed by the sample cutout bus 158 to the gates of the sample output transistions of the analog of the circuits of all the pixels 154 and the sample select transistor 152 is connected to the source of the sample output transistor 156. The gate of the sample output translator is con-The node between the sample storage capac to a constant voltage source, e.g., ground. constituting the pixel array 102.

10074] The drive signal generator 128 will now be described. The drain of the sample output translator 168 is comnoded to the electrode 159 of the ramp capeation 160. The electrode 161 of the ramp capeation is connocled to the RAMP signal generated by the ramp gan-eration 144 (Figure 4A) and distributed by the ramp has 162 to the ramp capacitors of the englog drive chours of all the pixels constituting the pixel array 102.

The inverter 166 is composed of the PMOS another and to the output of the Inverter, and the sources of which are nespectively connected to high and 10075) The electrode 159 of the ramp capacitor 160 is also corrected to the drain of the reset translistor 164 and the Input of the Invener 166. The source of the reset tarsistor is corrected to a constant voltage source. a.g., ground. The gate of the recet transistor is connecked to the reset control signal QLE generated by the dock generator 142 and distributed by the reset bus 168 to the gades of the reset translators of the analog of the transistor 170 and the NMOS transistor 172, the gates of which are connected to one another and to the Input of the invertor, the chains of which are connected to one low constant voltage levels V+ and V-. These constant voltage lavels may be, for example, the positive power drauts of all the pheat constituting the pixel array 102. 200 8 8

2077] The cultiput of the Invarian 166 is competited to mination selector transistor 176. The structure of the inverter 174 is identical to the inverter 166 and so will nected to the source of the balance selector transistor 178. The drains of the solostor translators 176 and 178 alctors 178 and 178 are respectively connected to the LLLAM control signal and the BAL control signal. The ILLUM and BAL control signals are generated by the he impart of the inverter 174 and to the source of the illunot be described. The output of the Inverter 174 is conre corrected to one another and, by the conductor 120, to the electrode 118. The gates of the selector tran-160 and 182, respectively, to the gates of the selector transistors of the analog drive circuits of all the phods clock generator 142 and are distributed by the busses supply and ground, respectively. \$

? common electrode 33 shown in Figure 2B espaceanably mid-way between the high and low con-80,00 constant voltage ŝ dant voltage sources. corrected to

Operation of the just-described embodiment of he spatial light modulator 100 according to the inven-

50, and 6A-6R and 7A-73.

EP 0 853 960 A1

inverter 168. During the following blanking period, the LED other supplies no current to the LEDs, and the dook generator generates the BAL control signal shown the LED driver 67 supplies current to the LEDs 69-71. The ILLUM control which connects the electrade 118 to the autput of the for transistor 178 ON, which connects the electrods 118 in Figure CD in its 1 state. This turns the balance seleceignel turns the Burnination selector trancistor 176 ON control signal in the 1 state whenever to the output of the inverter 174. will now be described with reference to Figures 4A firning daptams shown in Figures SA-

9 Figure 5A shows the basic operation of the above-described embodiment of the spatial light modu-lator in which analog samples of frame I are loaded during the picture ported of trame 1, and a display ples of frame 1 during the picture period of trams 2. The features of the victeo algoral are each divided into a varitpicture period of frame 1, an analog sample derived coeration is performed in response to the analog semcal blanking period VB and a picture period. During the from frame 1 of the video signel is loaded into the sam-ple charage expection 154 of the smallog drive choust of cooch pived in the placel amay 102. This process will be Simultaneously, a display operation is performed in response to the analog samples of the previous trame During the vertical bianking period of frame 2, the sample of frame 1 stored in the earrarie storage for of the pixel. Then, during the picture period of frame capacitor of each pixel is transferred to the ramp capac-2, a display operation is parturned in response to the aredog sample transferred to the ramp capacitor of each pixel in the pixel array. Simultaneously, an analog sambatow with reference to Figures 6A-6R ple of frume 2 is loaded into the sample storage capacllor of the pixel.

the LED driver 67 feats current to the LEDe 69-71 to The waveform of the current supplied to the shown in Figures 58. During each illumination period, period and the vertical blanking period precasing the to cause the pixel to modulate the Intensity of the light 69-71 by the LED other 67 is schematically cause the LEDs to ituminate the spatial light modulator 100. During the balance period following the illumination Burnination poriod, the LED offiver turns the LEDs OFF. During the illumination period, the analog orive circuits of all the pixets constituting the pixel anay 102 similargenerate the illumination sequence of the drive signal that they epply to their respective pixal decinates reflected by the pacel. During each balance period, in arabg drive draults of all the pholes simultanously gon-erate the beliance consenso of the drive signal. The balunce sequence of the drive signal is complementary to which the spatial fight modulator to not filuminated, the of the drive signal and estones the DC balance of the pixel. The office signal will be further described below with reference to Figures he illumination sequence ä

[1082] The wevelocins of the LLLIM and BAL control signals are shown in Figures 6C and 5D, respectively. During the vertical blanking period at the beginning of the coloctor translators 176 and 178 are OFF, and The voltage on the pixel electrode 118 is approximately equal to the voltage on the common electrode 33 (Fig. u.v.o.28). The chock generates the ILLIBM u.v.o.289. sach freme period, the clock generator 142 generates ooth of these control signals in their 0 state. Accordingly,

with relevance to Figures 44, 48 and 64-87. Figures 64-60 respondively show the control signal waveforms on the control lines 1391-1389, corrected to the control lines 1381-1389, during the picture frouts of the SM circul (10083) The process by which an analog sample of the age capacition 154 of the enalog drive circuit of each period of one frame of the video signal. Figure 6E shows an example of the waveform of the video signal frame of the video signel is loaded into the sample ctor pixel in the pixel amay 102 will now be described below Ye ted from the butter amplifier 198 to this signal inputs of the SAH circuits 1384-1384. Figures 6F-61 respectively fed to the column busses 1311-1314, respectively. In particular, Figure 6G shows the sample waveform on the column bus 131₂ connected to the sample input 150 tol signal on the control line 13% returns to its 0 state, the S/H drouit 13% holds the leval on the column bus afrow the sample outputs of the SM circuits 138;-138, of the analog offive circuit 114 of the pixel 112. Sampling begins when the control signal on the control line 139, goes to its 1 state. When the central signal is in this state the output of the SAH circuit 138, connected to the column bus 1312 follows the waveform of the condifoned vidoo signal shown in Figure GE. When the can-131₂ at the level of the conditioned video signal at the tersition of the control signal. The lavel on the column bus remains at this fevel unall the next time the control signal on the control line 139, goes to its 1 state ¼-way along the next line of the conditioned video signal. 8

[DOB4] Figures 6J-6M drow the waveforms of the control signals on the row select busses 1984-1384, respectively. Each of the control signels is shown as being in the I state for the duration of one line of the video signal, and is in its 0 state for the rest of the trame. However switch to their states at a firme later than the start of their nour sealect control signates

forms on the sample storage expaditors of the analog Figures 60-6R respectively show the wavedrive circuits of the pixels 184, 112, 185 and 186 in the socond row of the pixal array 102. Analog samples of the second line of the video signal are accepted by the cantrol eignal on the row select bus 133₂ connected to the pixel 112 to in the 1 state. The control signal turns the sample select transister 1.52 CN, which comeds he cample storage capacitor 154 to the sample input these pixels. During the second line of the victeo signial, As a result, the votage on the cample storage

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linely reaches a constant voltage when the output of the SM circuit chiving the column bus goes into its expactor first charges to the voltage on the column bus then follows the voltage on the column bus, and

22 8 Fitally, the voltage on the serrote spange capacitor contess a constant level consequently to the level had by the output of the SM chould 1885, at the end of the second quenter of the second fine. The voltage on the sample strage capacitor neadles this condition at the sample strage capacitor neadles this condition at the control dynal on the row select bus 133, changes to he 1 state at the beginning of the second line, the winage on the serrate strates capacitor 154 of the arealog drive. colum bus 1819. These voltage charges occur as a routh of the EAH aircan 1829, sampling the second quarter of the socond line of the conditioned wideo signal. orad 114 charges to the level on the columbus 131₂. The voltage on the sample storage capacitor then fol-lows the voltage changes, shown in Figure 6Q, on the 10086] In perfoular, as shown in Figure 5P, when the the of the falling edge of the control waveform shown in Fours 6B

on the sample storage capacitors of the places 184-186 in the second row of the array billow the changes in the Figures 60, 60 and 6R show haw the voltages

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ple dampe especial (54 from the sample signal 190, As a result, the voltage on the sample strange especial centure fined at the level it had when the control signal on the row selector has changed state, as shown in Figure 6f. The voltages on the sample strange capacitors as respecified, when the control algoral on the row selector but 133₂ (shown in Figure 810) is in its 1 state, and remain constant during the other three lines of the control eignal on the row selector bus turns the sample select translator 132 OFF, which disconnects the samvoltage on the column busses 131, 131g and 1314. mai, the control signal on the raw selector bus 1335, changes from the 1 state to the 0 state, in this state, the At the end of the second line of the video sigin the phasis 104-186 in the second row of the array also become fixed when the control signal on the row salocfor bus 1332 roverts to the 0 etate.

the control signal on the one of the row select busses During the other three lines of the video signal, 133, and 1334 corresponding to the line of the video signal recolved at the video input changes to the 1 stats. As a result, the voltages on the sample sample sample capacitors of the phoals in the corresponding row of the phas array follow the voltage levets appearing on the odurm busses 131,-131,. At the end of each line of the row of the pixel array reverts to the 0 state. This causes the voltages stored in the sample storage apacitors of the ploads in the row to remain facel units video signal, the control signal on the one of the row The processes by which the office signal genthe corresponding line of the next frame. [0090] — The processes by which the def ä

period and the balance period constituting the frame 1 display period shown in Figure SA, but with a different to Figures 7.k-7G and Figure 48. The drive signal has a sample and subsequently restores the DC belance of during the vertical blanking period and the illumination cample stored in the sample storage expection 154 1 state chration that depends on the value of the enalog the pixel. Figures 7A-7G show the events that occur time scale from that of Figures 5A-5D.

the output of the ramp generator is in its minimum state, as stoom in Figure 70, and both the ILLIM and BAL adjente on in their Ostates, so both selector transitors. The and 178 are OFF. Consequently, the voltage on the pibel electrode 118 is approximately equal to that on the [0091] Figure 7A echamatically shows the waveform of the current through the LEDs 69-71. During the variation common electricals 88 (Figure 29). At the start of the vertical blanking period VB, the reset signal shown in Figure 78 brishly turns the reset transistor 164 ON. The reset transistor discharges the analog cample of frame cal blanking period prior to the illumination period, no current flows through the LEDs, as shown in Figure 7A, O from the ramp capacitor 160, as shown et 187 in Figure 7E. The ramp capacitor is now ready to receive charge from the sample storage capacitor.

the output select control agreal SEL shown in Figure 7C evitches the sample output handson 166 CNL This connocts the sample expected 154 in perallel with the ramp capacitor 164 in parallel with the ramp capacitor 160, which is in a discharged state. [0082] After the reset transistor 164 has turned OFF, Cherge sharing occurs, and the vollage on the ramp ospacitor rapidity increases, as shown at 188 in Figure 7E. The voltage level to which the voltage on the ramp switches the sample autout transletor OFF et or betone the end of the vertical blanking period, as shown in Fig-ure 7C. This isolates the ramp capacitor from the samexpedien rises is proportional to the charge in the cample storage capacitor before it was connected to the ramp capacitor. The output select control signal SEL ple storage capacitor. 8 Ħ

age is indicated by the line 199 in Figure 7E. As a result, the cutput voltage of the inverter 166 continues in its high state, as shown in Figure 7F. However, show the [0093] Notwithstanding the increased voltage on the name capacitor as a result of the charge sharing, the voltage on the electrode 159 of the remp capacitor 160 is below the threshold voltage of the inverter 166 at the pixel electrode 118 is disconnected from the outputs of both inverters 168 and 174, the voltage on the pixel electrode 118 is approximately equal to first applied to end of the vertical blanking period. The threshold voll-\$

vertical blanking period VB. In response to the trailing adde of the vertical sync pulse marking the start of the

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LED drive (7) to feed current through fire LEDs 69-71 as statum in Figure 7.4, asis the ILLIM control signal to the Bir I state, and vigoses the name generator 144 to extrigeneeding the sump wavefum shown in Figure 57. [8085] The ILLIM control signals, shown in Figure 57. (2005) The ILLIM control signals, shown in Figure 57. (2007) The sate the electrode 118 to the output of the inverter 166. The sate the widage on the electrode in the vulture of the inverter 168 shown in Figure 77. (L. t. to the 1 state shown in Figure 73, and marks the state of the first lemposal portion of the Illumination period. The BAL control signals shown in Figure 63, shown in Figure 73, and marks the state of the first lemposal portion of the Illumination period. The BAL control signals shown in Figure 63, shown in Figure 63. Respix five bildurice select transistar OFF.

DOSSI The ramp bignal generated by the ramp generator 144 is applied to the electrod o 161 of the tamp capacitor 160. An the first tentocral portion progresses, the ramp signal causes the voltage on the electrode 153 of the ramp capacitor to include the voltage on the electrode 153 of the ramp capacitor to include 153 of the ramp capacitor to a 160 in Figure 70. At the point 191, the voltage on the electrode 153 of the ramp capacitor roaches in the restind voltage of the investiration at 150 in Figure 77. Show the carp capacitor roaches in the restind of the investiration of the 161 include 153 of 161 include 153 in Figure 75. Show the capacitor is about at 152 in Figure 77. This masks the end of the litter temporal portion and the beginning of the second temporal portion of the litter indian period. This parts electrode remains in the distribution period chown in Figure 75. This masks he end of the litter indian period. The property of the second temporal portion or the litter indian period. The masks of the litter indian period chown in Figure 74. The figure 75 his masks he end throached convenient in Figure 74. The masks of the second temporal portion canalism in the figure in the Eurithalian period chown in Figure 74. He second temporal portion canalism before 1 energies.

is connected to the output of the himertor by the illuminathin select branking if the voltage on the electronic as sizo dranges to the low state, as shown in Figuro 7G.

This marks the end of the first temporal portion and the bedyning of the second temporal portion of the illumination period continues in the fitting indich period. The price electrode remains in the fitting and research for the price acceptance in Figuro 7A.

100977. At the end of the illumination period, ramp sigpler of the second temporal portion constituting on the electronic 150 of the ramp capacitic sits quickly be level below the freshoal village of the hierare 158. This causes the output of the inverter 168 to resert to the facilities schown at 193 in Figure 7F. In addition, both the ILLIM corruct signal and the BML cortic against transfer the corruction for the price of against transfer the corruction for the pickle output of the inverter 174. The output of the inverter 178 CM, which transfer the corruction for the pickle output of the inverter 174. The output of the inverter 174 is in the 0 states when the output of the inverter 168 to in the 1 state. Accord— as 100 minute. The pixel electronic remains in the 0 states as shown in Figure 7G.

DOSS) When the level of the electrode 159 of the ramp depector neathers the Breschold vollage 188 of the lineate 166 order more, the outquit of the lineate 166 debrges state as schown at 154 in Figure 7F. The output of the hardter 174 also changes data, as a result of which, the voltago on the plate electrode 118 changes from the 0 debts to the 1 state, as schown in Figure 7C. This marks the earl of the first temporal portion of the butance period. The secured temporal portion of the butance period. The voltage on the place absolute of the butance

I state for the second temporal portion that constitutes the remarker of the behavior period mining largue YM 19099.

The starp weakom returns to be maintained state in the cord the balanceperiod, and the reset transtant in Foure T8 once more turns the reset transtant in Foure T8 once more turns the reset transtant in Foure T8 once more turns the creat transtant in Foure T8 once more turns to be 0 state and the LLUM control signal remains in its 0 state and the FLUM control signal remains in its 0 state, as shown in Foure SC and 50 et the end of the balance period. The debugle hit is state of the BML control signal isolates the plant debugle of the BML control signal isolates the plant debugle of the BML control signal isolates the plant debugle of the BML control signal isolates the balance once more, as shown in Figure 7A.

(IDTO) During the balance period, the drive signal has is in its 1 state for the second temporal portion that is is ornelementary to the first temporal portion in which the drive signal applied to the pivel electrole was in its 1 state during the itemination period when the sprise! State during the iteminated. Consequently, the wol-age on the pixel electrode 118 is set to the 1 state and 20 to the 90 state are quall portions of the display period so that the DC betance of the portions of the display period so that the DC betance of the special syndromial.

Fast the DC detance of the pixel is markened.
[8701] The duration of the first temporal portion of the librariant period in which the pixel elecande 118 remains the 1 state depends on the tistical voltage to 35 which the many expendent 160 was deregad by draing staining with the sample stanges especiater 154. The DC land with the sample stanges especiater 154. The DC land with the temple of the wideo signal 50, generalized by the tuthra carpliller 156, the voltage many signal and the mention of the sample stanges especiate control of an odd so that the inventor 156 changes state effects of the them fine voltage of the sample stange of the sample stanges especial come sports to the caralina of the operation strategies of the reverse consequence to the temple state with the earthet of the fluraisation period which the sample voltage is at the minimum of the observation serior of the dynamic respect the voltage size at

when the sample votlege is at the minimum of the dynamic range of the votes signal. Birtog! The budsen lines 168 and 197 in Figures 7F and 76 intraste the longer duration of the 1 states of the output of the inverter 168 and his past electrode 118 respondinely, when the level of the analog sample is lover, as industed by the brotom line 168 in Figure 7E. The oqually-broger duration of the 0 state of the post electrode in its billioning belance parind is britisated by the brotem in the 168 in Figure 7C.

the broken the 198 in Figure 7G.
[0103] in the stone-described embodiment of the aready drive force, and in the embodiments to be described below, the stages that drive the pinel elso trode are required to change state only twos per trame. The aready drive droughtes by the aready drive droughtes a burst power constrainted intern a eligital drive droughtes a burst power constrainted interned the electromach and the drive droughtes are a pure drive droughtes are a pure drive droughtes are a pure drive drought of the electromach and the driven droughtes are d

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electroto 118 during the Burnization period and the article storage capacitor 154 depends on the threshold voltage of the invariant 166. The threshold voltage is process-dependent, and can diffur between makins, between plans arrays on the came weier, and between the arrayd three choices in the same paid array. With current processing technology, these threshold voltage variations mink the groy-case recolution of the special informations. In this latest graphs and video applications require a large vegre-casio resolution of the states in this mink the groy-case resolution of the special voltage variations mink the groy-case resolution of the special voltage variations require a largey cyely-casio resolution in this.

(1916) Figure 8 shows a second embodiment of an analog drive directli flori includes the effect of threshold voltage variations, and that can threshon provide a grottler grey scale ternation. In the embodiment shown is h Figure 8, elements that correspond to those of the embodiment shown in Figure 48 are inclusived by the same reternor interests, and will not be described egain from The sample derivation and destrution eit. Call that provides areing samples ent come degrets to the orthodiment shown in Figure 8 is similar in that shown in Figure 8.

here.

[0109] In the embodiment of the analog drive circuit shown in Figure 8, the sample selection section 128 is the same as fait of the embodiment shown in Figure 9, the sample selection section 128 is the same as fait of the embodiment shown in Figure 48. In the other slope generator 120, the liquid of the inverter 168 is commercial to the electrode 159 of the marp capacitor 150 of the marp capacitor 150 of the marp capacitor 201. The drive signal gomentor additionally includes the caballocated to the toput and output, respectively of the inverter 188. The grain of the original control signal of the inverter 188. The grain of the original control signal OS CORR. The office correction control signal OS CORR. The office domestion control signal of the business of the original of the original of the original o

Invariant ISB. The gath of the officed connection transister is connected to the officed correction control algorithm (OOHR. The officed comescion control signal is generated by the clock generated vite and is distributed by the base 205 to the officed connection transisters at the arradig office distributed by the base 205 to the officed connection transisters of the reasts of all the plates consisting the pode intray ICD.

[VIOT] Finding, the source of the reset transisters (16) is connected to the reference signal SOLEAN. This reference eightal signal to the network signal SOLEAN. This reference eightal signal by the odoxt generator 142 and is distributed by the blue 21 to the sources of the reset transisters of the arreigo dive declarate of the reset transisters of the arreigo dive declarate of all the plates correlating the packs larray ICD. As shown in Figure SC, and the reference signal SOLEAN has two retacles of the reset invested of all the plates after 156 and a low state dose to the low votage for the reference signal SOLEAN was half-way between that and low votages of the reference signal SOLEAN was half-way between that and low votages of the reference signal SOLEAN was half-way between that and low votages of the reference signal SOLEAN was half-way between that and low votages of the reference signal SOLEAN was half-way between that and low votages of the reference signal.

1919) Operation of the entrodiment shown in Figure 1919) Operation of the entrodiment shown in Figure 48. However, at the beginning of the various barriers period VB of each ferme, the offset correction control styres US COPHs and the clear control signal CIE are asserted as shown in Figure 98 and 98, mapochwey, in addition, the reference apprail SCIEAR cuitables to the

high state V_{res} at the beginning of the verifical banking petic), as shown in Figure 9C. The older correction cartind signal burse ON the offset correction tearstar 20%, which intercorrects he input and output of the levents of the levents of the levents and which intercorrects he input and output of the levents and the levents and the levents and the vertage on the electrode 207 of the coupling capacity 201, precisely to the threstrod voltage of the levents 194 ON. The recel transfers corrects the clearing the Coupling capacity 201, precisely to the threstrod voltage of the levents 194 ON. The recel transfers corrects the electrode 209 of the coupling capacity 201 to the nest electrode 209 of the coupling capacity 201 to the nest energy and offset correction transfers together as it file voltage across the coupling capacity 201 to a value of equal to the difference believes the actual threshold voltage.

gitting Part-way through the vertical blanking period VR, the control signal ON CORR is de-assantal, as drown in Figure BB. This tumes the diset correction trensition of the signal ON CORR is the coupling apparature 201 emelline. Simultaneaush, or slightly late, the relevence signal SCLEAR evitations to bits but state. V. as shown in Figure 9C. Since the control signal CLE is slid asserted and the receip tumistion Yells is fift any expective (60 discharges to a low voltage state intrough the reset furnishion Yells in the name capacitor to discharges to the low voltage state intrough the reset furnishes. After a time sufficient for the name capacitor to discharge tubility, the control signal CLE is the descretched and the reset transfect 164.

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burs off.

(P110) After the escut translator 164 has turned off, the control egypat SEL is asserted, as shown in Figure 90. This turns the selector translator 159 ON Charge share, into between the sample exception 154 and the 50 tamp expectation 154 and the 50 tamp expectation 154 and the 164 ferror and plane 75. The control eights SEL is clease sented before the and the vertical banking period VB to leadable to tamp expected from the sample strange casualty.

or opporation of the drive signal generating eaction during the illumination and batance periods constitution. The display period is the same as that described above with reference to Figures 7E-70. When the ramp valleage is applied to the electrode 161 of the ramp capacitic ege is applied to the electrode 161 of the ramp capacitic readed on the electrode 169 of the ramp capacitic meades a voltage equal to the high state V₁₄₅ of the reference signal SCLEAR, irresponse of able treatment of the reference signal SCLEAR, irresponse of able true in the inverter 168. The earn will be true for the inverter of the inverter 168 increases the grey scale resolution of the inverter 168 increases the grey scale resolution of the inverter 168 increases the grey scale resolution of the inverter 168 increases the grey scale resolution of the invertice to greater than impubation according to the invertice to greater than impubation as

10112] The embodinent of the analog drive droublust described with reference to Figure 8 includes three expections. The area of efficien occupied by these

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repocitors using present-day standardon inchriques requesions a majority of the area of each arriang drhe charify and less than the number of poses that can be provided on a die of a plann size. Alba, the spetial light modulator is iturinated for a total of one had of the pip. It was period of the video size. Since the various banks they period is about 6% of the frame period, the lithmation afficiency is choul 46%, it would be otherated by horses the itemitistic elicitory of the special light modulator to the theoretical maximum of ne appetial light modulator to the theoretical maximum of ne

dorts. A second embodiment 214 of the unalog drive dorts according to the invention will be described near with reference to Figures 114 and 108. This embodiment performs simultaneous escrepte locating and departs operations, enables and includes y according, enables could confine you depart on 50% to be achieved, while requiring only two capacitiess per enable of the force. The number of capacities is reduced by eminating capacities to reduced by eminating capacities to reduced by eminating capacities to reduced by eminating a southorn to the inventor off. Set problem that does not require an excititorial espacities. Consequently, this entabliment can form part of a spaid light modernor having a greater number of positions 48 and 8.

ures 48 and 8.

(0114) Figure 100 stones the sample denination and distribution bindut 204 that derives arrabes samples from the video eighal received via the video by the total or the arrabig denination for the sample denination by proceedings by the binary. This cincia and be proceed constitution to the binds and and denination of the sample denination and denination of the sample denination and dentation received the sample denination and dentation received the sample denination and dentation forcial 104 few forms in Figure 44 are indicated by the same research on memoria and will not be described. Elements that are sample and will not be described. Elements that are sample and will not be described. Elements that are sample and will not be described. Elements that are sample or forward or decard of the arraphological of the odditions than selector 255 between the order of an odd there selection but and in contribute election but a for an event of phosis in the province of an odd there selection but and in contribute selection but a for several none of phosis in the province of the

election task for each now of posts in the paint emer.
[1916] A wall be described in more detail below with reference be Figure 105, the austral detail below with reference be Figure 105, the autory direction 2.02 has a searchesy post 2.12 in the poid army 2.02 has a sample asset (Prof.s. at many hybri, and and even-frame row select (Prof.s. at may hybri, and and even-frame row select (Prof.s. at may hybri, and and even-frame row select (Prof.s. at may hybri, and and my frame from a compensation entered signal to the prices in the remaining phasis constituting the phose in each column of the prices army elegion media of the prices in each column to which is con-rected to a respective column bus which is con-rected to a respective column to the prices in the first column of the pixels in the direction of the pixels in the direction.

bus 131., The location in each line of the vidoo signal from which the analog sample received by each column of pixels is defined depends on the may position of the column in the pixel surex.

(1916) The add-frame row select inputs of all the pixels in each row of the pixel array 202 are cornected to a respective add-frame row select buts, and the everythment or weeked buts, for example, the add-frame row select buts. For example, the add-frame row select puts, for example, the add-frame row select puts of the pixels in the second row of the pixel erroy in which the pixel so the second row of the pixel erroy in which the pixels in the second row of the row-frame row select buts 1930, and second row are connected to the add-frame row select buts 1935, and second row are connected to the accordance row select but sides. [6117] The code and ever-frame row select busses

50% and to reduce the number of expacitors to two per

enalog drive droug.

(011) The odb and eventrame tow elect bussess are connected to respective outputs of the oddieven frame selector 234. The oddieven frame selector 124 to oddieven frame selector 124 to oddieven frame selector 124 to a connects each output of the row selector 134 to a connects each output of the row selector 134 to a connects each output of the row selector 134 to a connects each output of the oddieven frame selector come is 132, connects the second output of the oddieven frame selector come is to the tryat of the oddieven frame selector come is to the tryat of the oddieven frame selector come is to the tryat of the oddieven frame selector come is to the tryat of the oddieven frame selector come is to the tryat of the outputs corrected to the codi-oddieven frame selector come is manufactor to the oddieven frame of the selector of the video degral present at the sample tryou select fructs is the 1 state, for example of the video degral present at the sample of the video degral frame of the row select busses to the 1 state and each examine of the video degral the row select busses to the 1 state of the addieven frame of the video separal are received these of samples can be received by the putals in the first an arrange samples can be received by the putals in the first

(bit) The oddleren trans celectrr 225 is composed of a pair of two-trait gates for each now of pades. The output of one of the gates for each now of pades. The output of odd-frame select that 1330, of the now and the output of the other of the gates is connected to the owner of the output of the other of the gates is connected to the owner of the first thou of each of the gates connected to the owner of the new number. A first thou of each of the gates connected to the owner of the first of the owner, the second trapt of the owner, of the owner, the second trapt of the other owner of the odd-frame control bus 237. The dark to the other owner, as or or or the owner, and the odd-frame control signals are generated by the cold generator 242. The odd-frame control agrees is the 1 tests, the seminated output odd-frame control agrees is the 1 tests, the seminated output odd-frame control agrees is the 1 tests, the seminated output of the owner, in the 0 tests of the video signal, and is in the 0 tests of the sideo drame control signal is the interest of the odd-frame control

(D119) With the arrangement just described, the odd/oven frame selector 235 maintains in the 0 state the

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out-1 and even-frame row edect buseas of all mass out-1 and even-frame row edect buse and the state. The states of out-frame row edect bus and the even-frame row select bus in the 1 state and the new edect bus of the out-frame control is in the 1 state before the state of the north-frame control is signal and the even-frame row select bus is in the 1 state only when the odd-frame control signal is in the 1 state only when the odd-frame control signal is in the 1 state only when the even-frame row select bus is in the 1 state only when the even-frame rows select bus is in the 1 state only when the even-frame control signal is in the 1 state only when the even-frame control signal is to the 1 state only when the even-frame control signal to be fold to the arrabog drive checks of the twice of signal to be stored in the odd-trame and even-frame serple read-don-conform, respectively, of the arrabog drive drive in the odd-trame and even-frame serple read-don-conform, respectively, of the arrabog drive drive.

described with reference to Figure 108. The analog himo 2280 sample selection conton, the even-frame sample selection section 228E and the drive eignal gon-erator 228. Both semple selection sections are composed of identical circults whose operations are fare multiplicated to maximize the Rumination officiancy of the spalls fight modulator 100. One of these duplicate cir-The analog drive circuit 214 will now be plary pixel 212 shown in Figure 10A. The analog drive draif can be regarded as being composed of the oddcuits receives an analog samplo of the ourrent frame of the video signal at the sume fame as the chive signal generator generates a drive signal in response to an analog sample of the previous trame stored in the other. diffe dirout 214 is the analog diffe circuit of the earn-The cooking semple selection section 2260 selects an analog sample derived from each odd frame stores this enalog sample in an even-frame storage of the video storal and stores the selected analog sam-ple in an odd-frame sample storage capecitor, and the even-trame cample selection seption 226E selects an emelog sample derived from each even scane and capacitors are atternately colected and led to the drive signal genomics 228 which generates a chive agnal in erator sequentially generates office signals in response capacitor. The analog samples clored in the storage to the analog samples derived from consecutive frames of the victoo signal. Each drive cignal generated by the drive signal generator additionally restores the DC tooresponse to each enalog cample. The chive algnal gen-(OZ 150) 922

ance of the pixel 21:2.
[D122] The acch feature sample selection section 2280 of the carebo drive droud 214 of the secentral rypad 212 will now be described. The over-feature sample selection section 228E is almost identical and will not be described. Corresponding stematis of the out-feature sample selection section section and the even-feature sample selection section and the even-feature sample selection section see Indicated by the same increase numerator with the letters 0 and E, respectively, actiod.

214 is connected to the column bus 1312, Also conmoded by a surple input is the drain of the serrable select trainstant 222.0, the gate of which is connected with the old row school from 2100 to the odd-framerow select bus 1330₂. The source of the sample select transtitut is connected to one electrode of the sample stateger capacitor 2540. The other electrode of the sample stratge capacitor is connected to a constant voltage level, eq., ground.

The node between the sample sounge capas 2520 is also connected to the source of the sample out-The gate of the carrole output transistor is connected to for 242 and distributed by the even control bus 239 to for 2540 and the source of the sample select transistor put transistor 2560. The drain of the sample output tranelator is connected to the Binput of the comperator 25% the control signal EVEN generated by the clock generathe gates of the eample output transistors of the oddframe sections of the analog of two circuits of all the pixels consilluting the pixal array 202. The sample output transistor 2560 is operated by the control signed EVEN because the odd-frame sample selection section 2260 feeds stored amilog samples to the drive agnal section 228 at the same time as the even-frame sample section and storage section 228E receives an analog sample from the sample input 250. For a similar reason, the ple selection section 228E is controlled by the control cample output transistor 236E of the even-frame samsignal ODD distributed by the odd control bus 237.

signal ODD distributed by the odd control bus 23.7.

(PULS) The comfort signal eVEN is selec convected to the gath of the ramp signal selector transistor 25.7.

The source of the ramp signal selector transistor is connected by the ramp signal selector transistor is connected by the ramp signal bus 213 to the ramp signal bus 213 to the ramp signal selector transistors of the arrange drive drunks of all the pixels constituting the point army 202. The detail of the ramp signal selector transistors of pixel army 202. The detail of the lamp signal selector parador 25.5.

257E is corrected to the Birput of the comprehen, and ment, aretag samples derived from the even fields of the sample storage capacitor 2540 are ted to the B The over-frame sample selection section 226E differs from the add-frame example selection section 255, the drain of the ramp signal sodector transistor the gatos of the trancistons 258E and 257E are conthe video signal and stored in the cample starage log samples derived from the odd framee and stored in right of the comparator and the namp signal is fed to the 2360 only in that the drain of the sample output transfe tor 256E is connected to the A input of the comparator nected to the OOD control signal, With this arrange capacitor 254E are fed to the A input of the comparator and the ramp signel is fed to the Binput, whereas ana-925 8

10/27] The other signal generator 228 will now be disorbed. The other signal generator includes the commentar 255 is a switched-tenso sentor 255. The comparator 255 is a switched-tenso

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section 228E and the offive signal generator 228 on are-23 the state of the comparator conso control signer SENSE the comparator sense bus 260 to the comparators of all the pixels constituting the pixel array 202. The comparator sense control signal serves two functions. First, the comparator sense control signal inverts the detaction constant delection serses with respect to the tamp sig-nal and the unalog samples despite the attenution of the connections of the ramp cignal and the analog sam-ples to the A and B inputs of the companior, For oddgenerated by the clock generator 242 and distributed by parator is conventional, and the output of the companithe detection some is inverted and the output of the companion in a 1 state or a 0 state, departing on whether the voltage on the B input is greater than, or loss than, the voltage on the A input. Second, the comsense of the comparator in the Numbration periods of successive frames. This provides the comparator with a framo analog samples, the detection sense of the comvoltage on the A input is greater than, or less than, the voltage on the B input. For even-frame analog samples, tor in a 1 state or a 0 state, depending on whether the

(0128) Alternating the inputs of the comparetor 255 to which the analog samples and the ramp signal are conneuted and haveling the detection sense of the compa-rator reduces the visibility of errors resulting from differences in the input officet vellages of the comparaillumination period. This enables the componator to generate the balance portion of the drive signal simply by darator sense control olgnal invents the detection sense of fire comperator in the ballance period latewing each repeating of the cycle of the ramp signal connected to tors. The inputs are atternated and the detaction sense of the comparator is inverted between consecutive over frame, the input offset adds to the ramp signal, so trames. For example, in an odd frame, the trout office may add to the enalog semple so that the pixel appears brightor than its nominal brightness, in the following the pixel expense dimmer then its nominal brightness. The trighter appearance and the dimmer appearance of the piral average between the two frames, so that the pixal expense et its monanal brightness. and of its imputs.

(0129) If the input office voltage of the comparator 255 is smed, or the input offset voltages of the comparature to the Ainput, for example, of the comparator, and conof all the analog drive circuits of the pival array 102 are similar, the analog drive circuit can be simplified. This the waveform of the comparator sense control signal should be charged so that the detection sense of the comparator is normal in the Kumination periods and can be done by eliminating the ramp signal solooton (randstors 2570 and 257E, connecting the ramp signal necting the drains of the sample output transistors 2580 and 256E to the Binput of the comparator, in this case, nverted in the balance periods.

The output of the compension 255 is connected o the pixel electrode 118 by the conductor 120.

cample and storage section 2500 and the drive signal generator 229 of the ambig drive chart on analog samples of the order numbered frames of the video signal. Figure 118 shows the operators sequentially performed by the eventrame sample selection storage. The offive signal generators shown in Figures 8 [0132] Operation of the enelogy drive circuit 214 of the exemplary pixel 212 will now be described with referpixel 212 is located in the eacond column of the second row of the pixel erray 202. Figures 11A-11O show the or 158 may be substituted for the drive signal generation waveforms in various parts of the carcuit in the course of bading analog samples of three consecutive tramps 1, 2 and 3 of the video signal into the sample selection sections 2260 and 226E of the circuit, and generaling ence to Figures 10A, 10B and 11A-11Q. The exemplary drive algrais in response to amalog samples of the prethe operations sequentially performed by the odd-frame vicus frame 0 and frames 1 and 2. Figure 11A shown 228 shown in Figure 10B.

bg semples of the even frames. Frames 1 and 3 are odd hannes, and frames 0 and 2 are even frames. 19153. As shown in Figure 11A, charge fibe frame 1 at sample lood partod, in which frame 1 is received at the widoo input 106 (Figure 10A), an energy semple of frame 1 is braded into the odd-frame sample electric secution 2280. The frame 0 display period shown in Fig-LEDs 69-71. The drive signal of the LEDs is exhemitically shown in Figure 11C. In the bedance period of the frame 0 display period shown in Figure 118, the drive signal generator generates a drive signal that restores ure 118 is concurrent with the Irams 1 cample load play period, the drive signal generator 228 of the circuit modulator 100 is illuminated with light generated by the period. During the illumination pariod of the frame 0 disgenerates a drive signal in response to an analog egmple of the previous teams, frame 0, and the spettel light the DC balance of the pixel, and the spatial light modulator is not fluminated. B

[0134] During the trame 2 sample load period shown irput 106 (Figure 10A), an analog sample of frame 2 is loaded into the even-bane sample selection section in Figure 11B, in which trame 2 is received at the video 220E. The frame 1 display period shown in Figure 11A ng the Bumination period of the frame 1 display period, generator generates a drive signal that restores the DC betance of the pixel, and the spatial fight modulator is is concurrent with the frame 2 sample load period. Durthe chive signal generator 228 generatas a drive signal in response to the analog cample of frame 1 stored in the odd sample selection section 2260, and the spatial ight modulator 100 is Iluminated with Rolff generated by display period shown in Figure 11A, the drive signal no LEDs 69-71, in the balance period of the frame 8

Finally, during the frame 3 sample load period shown in Figure 11A, in which frame 3 is received at the 9436<u>]</u>

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10A), an anatog sample of 3 is loaded into the odo-frame semple selection section 2260. The frame 2 display period shown in Fig. ure 118 is concurrent with the frame 3 sample load period. During the illumination period of the frame 2 cleplay period, the drive signal generator 228 generates a drive signal in response to the analog comple of frame 2 ated by the LEDs 69-71. In the balance period of the stored in the even szample selection section 226E, and the special light modulator is illuminated with light generales a drive signal that rectores the DC balance of the pixel, as shown in Figure 11A, and the spatial light modframe 2 deptay ported, the drive styrial generator gener ulator is not illuminated.

Figures 11D and 11E show the states of the periods that the odd-numbered frames are received at slightly asymmetrical to prevent the translators controlled by these control exprais belong ON simultaneously and to prevent charge sharing between the exportures ODD and the control eignal EVEN. respectively. The control eignal ODD is in its 1 atate curing the odd-frame sample load periods, i.e., during the The video laput 108, and is in its 0 state during the eventrame cample load perfoods, i.e., the periods during the even-numbered frames are received at the video input. The control signals ODO and EVEN are 2540 and 254E as a result. 9486) ş

Adeo cignal, an analog cample of the frame is loaded The artifog surples from the octs frames of the victor eightl are loaded into the odd-frame sample selection section 2250 of the artifog differ directi in response to (01377 In the sample load period of cach trame of the nto the analog dive circuit 214 by processes similar to the odd-fizmo row select signal. Figure 11F shows the els located in the sociand row of the pixel array 202. The ple reflection socitons of the analog drive circuits of only hose described above with reference to Figures 6A-GR. odd-frame row select eignal led via the odd-frame row select has 1330, to the analog drive charits of the pixadd-frame row select signal causes the add-frame samthe pixels toocted in the second row to accept the enelog serraies from the column busees 1811-1314, and corresponds to the row select clipnal shown in Figure 68. However, as can be seen in Figure 11F, the oddframe row select signal is only associated during the sam-Figure 11G shows the even-frame row salect signal fed the pixal emay 202. The waveform of the even-frame row select signal is the same as that of the odditume row select signal shount in Figure 115, detayed by one frame pile load perfeds of the odd frames of the vidoo signel. via the evon-frame now select bus 133E₂ to the enabo drive circuits of the pixels located in the second row of select signal is the same as

furtifier of one line of the video eignal, and is in its 0 Each of the row select control signals is shown 11G as being in its 1 state for the state until the corresponding line of the neet add or evan rame. However, the row solect control signals may in Figures 11F and 948

Figure 11H shows how the voltage on the oddfarme cample storage capacitor 2540 of the serging drive citals 214 dianges during the sample load perods of frames 1-3. Initially, the voltage on the sample storage capacitor corresponds to the analog sample of the beloe-previous framo (frame -1, en ood frame) of the rideo signal, as shown at 261. Then, the odd-brame row select signal shown in Figure 11F is asserted cluring the second the of hame 1. This eignal causes he somple capacitor 2540 to the column bus 1312. After a delay apparator continues to hald a voltage corresponding to select transistor 2520 to correct the sample storage corresponding to one pixol, the analog sample come eponding to the second pixal of the second line of the corresponding to two more pixels, the odd-frame for select signal is de-essented, which causes the eartple capacity from the column bus. The sample storage frame it is fied to the sample stonage capacitor. This Gauses the voltage on the capacitor to change to the level, as indicated at 263 in Figure 11H. After a detay the analog sample of frame 1 until the odd-frame now colect signal shown in Figure 11H is next asserted during feame 3. Then, the cample stonage capacitor ecocycle an analog sample of frame 3, as shown at 265 in Figure 11H. æ

During the even frame sample load periods, the even-frams row select signal fed via the even-frame row select bus 1935; to the analog drive droubs of the pixobs located in the second row of the pixel array 202 is asserted, as shown in Figure 11G. The even-frame row sided signal causes the even-frame sample selection sections of the analog of the cacatis of only the pixels boated in the second row of the pixal enay to except changes during framer 1-3. Initially, the voltage on the enalog camples from the column busses 131,-1314 Figure 111 shows how the voltage on the cample storcapacitor 254E of the analog drive circuit 214 Ine of frame 2, as shown in Figure 11(9. This eignal causes the sample select translator 252E to connect fre eample storage capacitor 254E to the column bus 191₂. Setretie corresponding to the second place of the second This causes the voltage on the capacitor to change to the column bus. The sample storage coparator continues to hold the voltage corresponding to the analog sample storage capacition corresponds to the analog sample of the provious frame (frame 0, an even frame) of the wideo algoral, as shown at 267. Then, the evenrame now select eignal is asserted cluring the second The of frame 2 is fed to the cample storage capacitor. one corresponding to the analog sample, as indicated at 269 in Figure 111. After a dalay comagonding to two Atter a delay corresponding to one pixel, the analog more pixels, the eventuame row select signal is deasserted, which ceuses the semple select transistar ₹ 2 8

states at a time later than the start of switch to their 1

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EP 0 953 960 A1 through the rest of the sumple load perfods of

hames 2 and 9 until the even-freme row select eignal is

critical. The rump eignal may begin in a high state and decrease towards a low state. Moreover, the ramp signal may begin in the low state and encrease towards the high state duving the flumination period and may then decrease towards the may state in the following belance drive signal in response to the ending earning of the pre-vious fearns loaded free one of the sample selection socions 2260 and 226E during the sample bad period the drive signal generator 228 generates the Figures 11J-11O show how, in each frame of the ramp signal RAMP, in the exemple shown, the the drawings, but a non-finear characteristic is pro-formed. A non-linear characteristic entatins gamma con-rection to be ponformed, as discussed above. The rearp of the previous frama. Figure 11J shows the waveform oqual to ons-half of the trans period. A ramp signal with linear voltage time characteristic is shown to shapility tamp signal has a sourtooth waveform and has a perion signal is shown in Figure 11J as boginning in a fow state and increasing towards a high state. However, finis is not ned essented in the next even frame 4 (not shown).

Figures 11K and 11L respectively show the vollage on the A and B inputs of the comparator 265. In EVEN changes to its 0 state, as shown in Figure 11E, and turns the sample output fransism 2560 and the range signal selector transism 2570 OFF Corseaddition, broken lines show the waveforms of the porthons of the ramp signal fed to the other input of the comshown in Figure 118, the control signal ODD shown in Figure 110 charges to its 1 state. This turns the sample output transistor 258E and the namp signal selector. rancistor 257E ON. At the same time, the control signal he compension 255, as shown in Figure 11K. The namp perator. At the start of the frame 0 Dumination ported quertly, the analog sample of the previous frame 0 stored in the cample storage capacitor 254E of the even cample selection section is connected to the Airpaul of ramp signal is also shown as a broken line in Figure agnet RAMP is connected to the B Input of the comparatur, as shown in Figure 111. The waveform of the Or wice versa. 142

[0143] Since the level on the Atrout of the comparator is willally higher than that of the B input, the nortinal output of the compensity is a f, as shown at 271 in Fig. sertee of the compension is normal and the drive signal convected to the pixel electrode 118 is in the 1 state for The ramp signal RAMP increases as the frame O Rumination perfed progresses. When the ramp signal use 11N. The comparator some control signal SENSE shown in Figure 11N is in its 1 state, so the detection the duration of the first temporal portion of the Illumination period, as shown at 273 in Figure 110.

to a 0. This marks the end of the partion shown at 275 in Figure 110. The second temporal partion constitutes the remainder of the frame 0 library temporal portion of the Burningtion period. The electrods remains in the O state for the second tempora 118, change irom a 1 b first temporal portion mination period.

trade remains undranged during the first temporal portion of the balance period, as shown at 277 in Figure [Df.45] At the beginning of the frame 0 betance period shown in Figure 118, the level of the namp signal RAMP shown in Figure 11J returns to zexo, and the nominal output of the comparator 255 shown in Figure 11M changes state, Howevor, cince the comparator sense control signal SENSE also changes state, as shown in Figure 11N, the actual output of the comperator remains unchanged. Consequently, the state of the pixel elec-

The ramp signal RAMP once more increases as the frame 0 belance period progresses. When the camp signal stightly exceeds the voltage of the sample clonge capacitor 254E, the nominal output state of the rator sense combol signal remains unchanged, the state of the pixel electrode also changes from 0 to 1. This marks the end of the first beraporal portion of the balthe secod temporal portion, a shown at 279 in Figure 110, constituting the remainder of the balance period. The spotsal light modulator is not illuminated during the comparator 255 changes from 0 to 1. Since the compaance period. The electrode remains in this state during Ibalance period. The states of the drive waveform in the first and second temporal portions of the balance period portions, respectively, of the illumination ported so that are apposite to those in the first and second temporal the DC balance of the pixel is restored. æ

to its 1 state. This tums the semple output transistor 2550 and the earp agaral selector harmstare 2570 of the outburness semple selection sociation 2250 Okt At the same time, the control agrael ODD changes to this ottak, as shown in Figure 11D, which turns the sample connected to the B input of the comparation 255, as shown in Figure 11L. The ramp signal RAMP is connected to the A input of the comparation, as shown in (DHT) At the start of the frame 1 illumination period, he control signal EVEN shown in Figure 11E changes output transister 256E and the namp signal solector transistor 267E of the even-frame sample selection secfon 228E OFF. Consequently, the sample storage capacitor of the cold sample selection section, in which en anatiog sample of trame 1 was stoned cluring the frame 1 sample load period, as shown in Figure 11H, is Figure 11K. The waveform of the ramp signal is also shown as a broken time in Figure 11L

nal curput of the comparator is 0, as shown at 281 in Figure 11M. The competator conse control eignal SENSE shown in Figure 11N is in its 6 state, so the detection sense of the comparator is invested, and the Since the level on the 8 input of the comparator 235 is initially higher than that on the A input, the norm-\$

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Sample storage

alightly exceeds the voltage of the

color 255 and, hence, the state of the posel electrode capacitor 254E, the nominal output class of the compa2

bkel decisions remains in the 1 state during the first in communication period, as an abstract and period, as an abstract and 18 the 110.

D149) The ramp signal increases as the frame 1 ithmination point progresses. When the ramp signal signey reseals the voltage stored in the sample stoage capacitar 2544. The normal output of the compantor dranges from 0 to 1 and the state of the pixal electrode charagos from 1 to 0, as shown at 286 in Figure 1(0). The electrode remains in this state for the seord temporal portion constituting the emainder of the farme 1 flurritation period during which the squital light modulation is flurritated (see Frame 110).

moddator is Burnheriad (see Figure 11C).

(9180) At the beginning of the frame 1 balance period, the level of the ramp signed FAMP intume to see, and is the forminal output of the comparator 255 shown in Figure 11M should be compared as the comparator sense composite strenges from 1 to 0. The comparator sense composite strenges from 0 to 1, so the state of the pixel electrods instructed professor (and opposite to that during the first temporal portion) during the first temporal portion of the selfence period, as shown at 287 in Figure 10.

portion of the belance period, studing the first temporal portion of the belance period, as shown at 237 in Figure 110.

[PUF61] The ramp signal increases as the thame 1 belance period progresses. When the ramp signal significance before progresses. When the ramp signal significance before by the comparator source or the display a few comparator. See shown in Figure 114 changes from 0 to 1. Since the paral electrode ented change from 0 to 1, as shown at 289 in Figure 114. The paral electrode innative in the paral electrode innative at 289 in Figure 114. The paral electrode innative in the paral electrode innative period. The special light manufactor of the farmer inblance period. The states of the drive merelorum in the first and socord temporal purfors of the between period are quancile temporal purfors of the between period are quancile temporal purfors of the between period are quancile to those in the first interval on period so that the DC belience of the paral electrod.

described. During the frame 2 illumination period, the [0162] Operation of the analog dive circuit 214 during the frame 2 Wuniscision and balance periods is the same as during the frame 0 flumination and balance respectively, and will thanelone not be analog other charif applies a drive signal to the pixel electrode in response to the analog sample of frame 2. The analog semple was stored in the cample storage It can be seen from Figures 11K and 11L that ing which the drive eignal applied to the electrode 212 is capacitors during the previous frame. The analog samthe tinst temporal portion of the illumination period, durin the 1 state, depends on the level of the analog cample docted in the respective one of the sample storage log samplo of frame 2 has a relatively high larel. The rediction of the filtumination period constituted by the first capacitor 254E during the frame 2 sample load period. ole of frame 1 has relatively low level whereas the are-

terrporal portions during the frame 1 Burniversion period and the frame 2 Burnitession period, respectively, in responsive the fortiers unalego samples deponds on the least off the artifoly samples.

10154) Figure 12 shows an example of a circuit first ray be used as the swached-serves comparent 255 in the susked drive circuit 214 shown in Figure 108.

Vertical Compositor 25% is composed of the convertical composed of the convertical composed at 11, the cuput of which is ket to convertical composed to 11, the cuput of which is ket to convertical composed of the convertical convertic

samples instructed about them. Moreover, comparing Figures 6D and 6J-6M shows that the control signel on each of the row select busses 133,-133, is 40-essented tical embodiment, the column busses are long and have substantial expedience and therefore obtay the analog for described above, the analog samples are distributed to the pixels by the column busses 131;-131;, the passalmost at the same lime as the last analog sample of each line of the video signal is placed on the column bus to be loaded into the analog drive circuits of the pixels at the right-hand side of the pixel array. The problem is sumpling arout 182, i.e., the pixels in the upper right of the pixel array in the oxemples shown in Figures 4A and derhadion and distribution circuit shown in Figure 4A and uses the analog drive circuit shown in Figure 4B. The embodiments shown in Figures 10A, 15A and 18 [0156] In the embodiments of the special light modula-1314. This, together with the transmission delay on the column busses causes less than the full analog sample especially severs in the pixels that are remade from the aut shown in Figure 19. The embodiment shown in 10A. The problem can be overcome using the embodiment 304 of the cample derivation and distribution cir-Figure 13 is a variation of the enthodiment of the sample can be similarly modified. 8 R 13 ş

W157] In the sample derhellon and distribulion drout at 304 shown in Figure 18, the now eithed busses are browned and the cards of the pivel sings to hom two eats of row select busses 1381—1881, and 1884—1883, and 1884—1883, and 1884—1883, and 1884—1883, and 1884—1883, are bornected to the now select pruss of the analog office drouts of the cards of the bandog office drouts of the early (columns 1 and 2 in the cerample shown) and to the output of the left-hand row select busses 1884—1838, are connected to the owe select busses 1888—1838, are connected to the owe select busses 1888—1838, are connected to the pixes in the offich-hand row select by the order of the pixes in the setting of the pixes in the setting of the pixel of the pixel of the droup of the inght-hand row selector 1348. The left-hand and right-hand row selector 1348. The left-hand selector 1348 described

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Above with retarence to Figure 41, and so will not be described again here. The chock signal LINE, described above with research to Figure 44, is fed to the chock input of the left-hand now selector 1341, and is also fed with the half-fire delay 135 to the right-hand now selector.

(0158) Operation of the cample denhation and distribution dring shown in Figure 13 will now be described with naturence to Figures 144-147. Figures 144-140 respectively phave the control signed wereforms on the control lines 139,-139, domenical in the control incurs of the 58H dirusin 139,-139, during the pickure period of one term of the video dignet. An enelog sample is pleaded on the respective column bus 131,-131, at each stalling odgo of these unwedoms.

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(0189) Operation of left-hand row salector 1841, is identical to that now salector 134 described above with reference to Figure 6.1-644. As above in Figure 145, the control signal on the row select bus 1334, switches to its 1 fatile at the beginning of the first like of 189 without of the first like 1 howers, during the second half of the first like 1 howers, during the second half of the first like 1 howers, during the second half of the first like 1 howers, during the second half of the first like 1 howers, during the semple-marked clubs in scrapbly, six performed by the sample-marked drukes 1884, and 1385, whose outputs are saidly drive circuits in the first low of the pixel of circuit comoded to the now select bus 1334, Accordingly, the armoded to the now select bus 1334, have to time corresponding to about cre-half of the line plant to receive the first services.

auty's fro analog drive circuits in the first low of the pixel analy that our connected to the row select bus 1884, have a time connected to the row select bus 1884, have a time connected to be sould one-shall of the line period to receive their sepactive custing surrises.

Dividij Operation of right-hand row selector 194 described stones with reference to Figures 64-64th, but its debyed by one-half of the line period. As shown in Equie 145, the control of the line period. As shown in 1634 is in its to select half of the line period. The drawys to the video signal, and drawges to the state had very through the first line period. The drawge in state takes placing his first line period. The drawge in state takes placing any stradog curripos of the first line of the video signal onto the column busces 1815, and 1916. Consequently, the creating three drawings in the first row of the place curry that are connected to the row educt bus 1831, are also the real of the video signal when the searches of the first line of the video signal when these sensing samples are put on the serroscoting because as e put on the consequently.

respective oxium busses.

(Intel) The row select bus 188H remains in its 1 state for the first fill or the video signal, and for the first fill or the second for the first fill or the second file, no sampling is performed by the sample-end-bod craute 188g, and 138g, whose oxiquits pre-corrected via file oxium busses 131g, to the arrange-end-bod file, no sampling the performed by the sample-end-bod file, no sampling is and 131g, to the arrange draw select bus 188H; Accordingly, the enabling draw clother in the first row of the pixel arrange first file connocted to the row select bus 188H; have a firme corrected by the first row of the pixel arrange first file connocted to the row select bus 188H; have a firme corrected to the row select bus 188H; have a firme corrected to the row select bus 188H; have a firme corrected the analog samples.

19162] The row setectors 1341 and 1341 operate in a manner strater to that obscribed during the remaining thes 2-A of the frame of the Video signed.

(0162) In the example chorm, he row select buses are behone symmetrically. However, this is not chickely be to row select busses may be broken asymmetrically with an appropriate change to the delay of the delay module 185. For example, the circuit row be configured to that the right row selector 194P controls only the arrange drive change becaute mod as a manage drive change because their analog sample in the would have insufficient time to receive their analog samples it they were controlled by the left row selector.

10164) In the examples shown in Figure 14E and 14E, coach output of each now selector is in lie 1 state for one states at the beginning and mid-point, respectively, of firely, of line 1. Moreover, these control signals are shown as reverting to their 0 states at the end of line 1 and the mid-point of line 2, respectively. However, as long as these control signals remain in their 1 for longer tine period. However, this is not critical. The control etg. nals on the row select busses 133L, and 133R, are shown in Figures 14E and 14F as switching to their 1 line 1. However, the row select control signals may switch to their 1 states may switch to their 1 states at a time fater than the beginning and mid-point, respeclino 2, respectively. The setting time of an arralog drive than the longest sealing time of the analog other dirouts revent to their 0 states some time before the end of line 1 and the mid-point of chast is the time required for an analog sample to transfor fully to the enabg drive circuit from the cample-and-hold circuit to which the analog drive circuit is conconnected to from, they may 9 8

hectod.

20 (1618) An example of a color display device based on the embodiment shown in Figures 4A and 4B is shown in Figures 4A and 4B is shown in Figures 15A and 16B is which elements corresponding to the total corrections is shown in Figures 15A and 16B, the earthol election election 2B of the examplery enalog dave circle 3H includes three sample should dave circle 3H includes three sample devication 15AR, 15AG and 15AR, one for each component of the color video signal. The papaller sample derivation and deshutton circle 4OA papaller sample derivation and deshutton circle 4OA one for each color component of the color video signal. The samplery circles was take enalog samples from one color component of the color video signal and devitous the enalog samples to the respective sample as those to durin busses for each column busses for each column in the pate array 102. The column color component dependent column busses for the first column of the pixel array are 191R, 191G, and 191B, to example.

1918, 1916; and 1918, for example.
19166] Interden eigene geverand 200 file analog
drive drutt 314 shown in Faure 1988 fro example output
remaisture 1889, 1660 and 1689 operate in response
to the exquentfally-extprilled select control eignals
to the exquentfally-extprilled select control eignals

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respectively, to sequenfielly

connect the analog sample stored in the cample storage equation 1941, 1940 and 1948 to the samp opposition for any throne when opposition for any visco signal processing opposition of the analog opposition of the analog opposition of the analog opposition of the draw signals, one of the furnitation period of coach of the draw signals, one of the LEDs 69-71 furnitation the quality in the draw signals, one of the LEDs 69-71 furnitation signal full modelers with light of a different order on responsibly to the odd-component form which the errain responsibly to the code component form which the errain of greater that of the opposition of the second often order of the prize is restored. In this embodiment, the digulaty portion for each often has a duration of one-stiful of the picture period of one frame of the code video signal.

[0467] The drive eignal generates 228 shown in Figure 158 may incorporate the offset correction droubly show in Figure 8.

R 8 B \$ (0188) The preferred embodiment of a color deplay device uses the parallel sample devicement distribution and distribution area (40 shown in Figure 154 but with the emalog drive chaut 414 shown in Figure 15C. The sample selection section 326 of the analog drive chaut is the 255 of the drive signal generator 228 of the analog drive same as that of the enalog drive circuit 314 shown in igure 158. The drive signal generator 428 of the enatog drive circuit 414 incorporates the sample output transistore 156R, 158G and 156B of the other signal generator 328 shown in Figure 15B and the input change-over circuity and entitable-sense composator diault 214 shown in Figure 10B. The Input change-over abautity, composed of the transistors 2560, 2570, 256E and 257E and the control signals ODD and EVEN, is respectively to sequentially connect the enalog sample stored in the sample storage capacisons 154R, 154G and 154B to the input of the comperator via the hour common node of the sample output transistors 156H, 1560 and 1568 on one hand and the hours A and B of disposed between the ramp signal bus 262 and the for comparation 255 on the other. The comple output ransistons operate in response to the sequentially-exppifod select control signale RSEL, GSEL and BSEL,

[0169] The input change-over circuity operates in response to the control eigrate EVEN and ODD. These curried deprins denige entitle in antiphrase between odd-introde and even-turbeed frames of the widoo signer. The control and even-turbeed frames of the decircuity and its large above the description sense of the comparator to take account of the action of the input change-over circuity and to hwort the sense of the comparator between the flamination provide and the belief or comparator between the flamination provide and the belief or comparator severage out in consecutive fearner, as decorative severage out in consecutive fearner, as flaminative and extrantions.

[0170] An exampto of a serial-load europic derhetion circuit 304 for use in a cofor display device based on the embodiment shown in Figures 10A and 10B is shown in

Figure 16 in which elements corresponding to the entrodriens shawn in Figure 104 are inflated by the same reflected runneab. In the entrodrient shown in Figure 16, the arealog drive clouds of the prizes is then best for the entrodrient strong in Figure 108, and will not be described further. In the sample deriver for and distribution clouds 504, the RQB sequence 211 corrects the color video signal to a color-sequential video signal in which the three color components of each frame of the color video signal are concentrated as further of the color video signal are concentrated as further of the color video signal are concentrated as further of the color video signal in the RGB sequence of as further of the color video signal, the RGB sequence 211 may be simple or more complex.

In [017] If the graphics adaptic is capable of generating a color-exquential video signel, the RGB esquence is a conventional to agaptics attained is a conventional graphics attained as them exist of grader than about 100 Hz, for cample, and interests on grader than about 100 Hz, for cample, and interests on the base of grader than 180 Hz, the RGB sequencer can be a three-way suith. The emith sequencial sedests the red, green and bus cotto components of consociation frames of the cottor video aignel. The emith sedests the red is consponent of all first frame, the green component of the cotor-coquential video signal. The emith sedests the red is consonent of the second items and the third frame, the second items and the third frame, as the first frame, the second items and the third frame, as the first frame, the second items and the third frame, as the first frame, the second items and the third frame, as the furth frame of the color-video signals. The sequences then repeats, the restor-video signals are furth frame of the color-video signals.

In 173 If the graphes extent is not capable of a high featin rate, the RCB sequence 211 samples each oxion component of each frame of the color video signal. The samples forbwed from each of component are temporated from each oxion component are temporated from an esquentially read out in color component order with a choic speed of three times the chiphal sampling rate can be used, and two or every times employing rate can be used, and two or every times samples not read out. The resulting color sequential this tratem is then subject to digital to unable conversion to generate to the calar-sequential video signal or made conversion to generate to the calar-sequential video signal.

(0173) The sampling chout 122 takes analog samples 242 and feeds the enalog samples to the column busses, in a time corresponding to the frame period of from the color-sequential video signal at the rate of the rate of the pixel clock generated by the clock generator The color video signal, each pixel of the pixel array portding to the three odor components of the frame of the color video signal. After an enelog semple of each frame of fine color-sequential video signal has been totaled into one of the sample selection sections of the receives a sample derived from each of these consecu-Eve frames of the color-sequential video signal comeanalog drive circuit of each pixel considering the ptxel 202, the waveform generator of the analog drive è 9 8

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retes the spatial light modulator with light of a color cor-responding in the color companient from which the a reading cample was derived, in the belance period of the display period, the dive signal restince far DC balance of the pixel, in this embodiment, the display pointed has a duration equal to the frame period of the colorlog semple. During the illumination period of the display draft generates a drive signal in response to the anaperiod of the drive signal, one of the LEDs 69-71 libraria

55 docorbed with various exemplary logic states, signal states, transistar types and rows and columns, the Although the above embadiments have been embadements can have apposite logic states, signal soquential victeo signet. **1**

Although this disclosure describes Mustrative embodiments described, and their various modifications stood that the invention is not limited to the precise hay be practiced within the scope of the invention embodiments of the Invention in detail it is to be underclates, transistor types and rows and columns. Seaned by the appended daims. 5175

R An smalog drive circuit (114, 214, 314) for othing a bkel electrode (118) in response to an analog sample demed from a video eignal, the analog drive orcuit comparising:

8 a sample selection section (128, 2250, 229E, 325) that receives and temporarily stores the ample curring a semple band period;

ශ් 4 Bequence of a first temporal portion and a sec-ord temporal portien, the tirst temporal portion and explies the dates signel to the pixel also-trode, the drive signel being composed of a 8 drive signal generator (128, 228, 328, 428) that, during a display parted that tollows the sample load poriod, gonerates a drive signal having a time duretion substantially proporbornal to the auralog cample temporarily stoned n the sample selection section, the sacand lemporal portion being a temporal complement of the first temporal portion.

The analog othe circuit of oleim 1, in which: d

analog sample only when the analog sample is the vitteo signal is composed of alternating odd no analog drive circuit additionally comprises the sumple selection section is an odd sample selection (2260) and receives and stores the and even trames each having a frame perfoct. aden from one of the odd frames;

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oven frames; and

nal in response to the enaby earnine stored in the odd sample selection section, end, cluting a display period coincident with each sample load period in which the analog sample is taken during a display period coincident with each generator generates the drive signal in response to the analog sample temporarily is taken from one of the even frames, the chive signal generator generales (228) the drive sigsample load period in which the analog sample from one of the cool frames, the office signal stored in the even sample selection sociton.

The analog drive circuit of claim 1 or 2, in which the video signal la a cofor-sequential video signal.

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The enelog orive circuit of claim 1, 2 or 9, in which The Chine signed generator operates in response to a remp signed that has a non-finear slope to provide gemma comection The enaiog drive drait of any one of claims 1-4, in which the sample storage section (126, 2260, 2265, 326) includes:

*6

a sample selection gate (152, 2520, 252E, 152R, 1520, 152B) that opens during the samof elond period to actnit the analog sample to a cample storage element (154, 2540, 254E, The sample storage element and that is closed during the display period; and ISAR, 1540, 154B);

(b) prior to the display period, the sample out-put gate being disposed between the sample storage of ement and the drive signal generator 158G, 156B) that opens one of (a) during and a sample output gate (158, 2560, 256E, 156R, 128, 228, 828)

The analog drive circuit of any one of claims 1-5, in į the drive signal generator (228) includes a comparator (255) that generates the other sigral, the comparator comprising a first input (A) to which a ramp signal is connected, the ramp signal having a clura-tion equal to the deplay period, and a secont input (B) to which the sample selection section is connected; and

when the analog dive circuit includes add and the analogichte circuit additionally comprises a switching element interposed between the aven sample selection socions (2260, 2265), sample salection sections and the second input

> en even sample selection section (226E) that receives and startes the analog sample when he analog sample is taken from one of the

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the odd sample selection section and the even sample relation section to the second input of of the comparator, and elternately correcting the comparator in consecutive display periods 7. The emelogicative circuit of any one of claims 1-6, in

the drive signal generator (128) includes:

an invortor (166) that generates the drive agnal, the treater having an input and an especialor (160) having a first electrode

(158) and a second decirode (161), the section (126, 825), the second electroda a reset swatch (164) that discharges the lirst electrode boing connected to the input of the inverter and to the sample selection 2008 citor prior to the display period; end being connected to a ramp signal, and

8

8 when the analog drive drass includes odd and he analog drive circuit additionally comprises a tion section and the even sample refection sec-tion to the first electricial of the capacitor and ewithing chament (2560, 256E) interposed between (a) the sample solection sections and (b) the first electrodo of the capacitor and the alternately connecting the odd sample saleooven temple selection sections (2260, 226E), input of the inverter, the substring element the input of the inverter in consecutive display

8. The analog office circuit of any one of claims 1-5, in

6 he second temporal portion is a linst sequence BALANCE) of the first temporal portion, in the sequence of the first temporal portion and erates the drive signal in a first electrical state (a.g., ILLUM) of the first temporal portion and the second temporal portion and has a duration the drive signal gonerator (129, 228, 328) genduring the first temporal portion and in a socfonally composed of a second sequence (e.g., which the drive signal is in the second electrical and the second temporal portion, in portion, and generates the drive signal addistate, the Met temporal portion and the second tamporal portion being in any order in the eecand electrical state during the second tempora which the other agnel is in the first electrical oqual to one half of the display period; and

a first impur (A) to which a ramp signal hav-ing a chradian equal to one-half of the cis-play period is cornected, and

a second input (B) to which the sample when the enabg drive circuit comprises odd and even sample selection rections (2260, 226E), the analog drive circuit additionally between the sample selection sections and the a switching element interposed second input of the comparator, the suitching element alternately connecting the odd sample selection section and the even sample selecdon section to the second input of the comparasalaction section (128) is connected, and for in consecutive display periods. comprises

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The analog office circuit of claim 1-5 or 8, in which:

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the drive signal generator (228) includes a nal, the comparator comprising a first input (A) sense set by a sense control atonal (SENSE) comparator (255) that generates the drive sigand a second input (B) and having a delection having opposite states in consecutive display the analog drive circuit additionally includes: periods; and

elternately connects a namp signal to (a) the first input and (b) the second input of a first switching element (2570, 257E) that perfods, the ramp signal having a dustion nacts the sample selection saction to (a) the second input and (b) the first input of salection sections (2260, 2265), a second switching element (2560, 2565) that absethe comparator during consecutive display when the analog drive chout comprises a switching element that effermately conthe comparator during the consecutive deplay periods, and, when the analog drive choult comprises odd and even sample nately connects (a) the odd sample selecsection to the second imput of the water and (b) the even sample seleesingle samble selection section, a second ecction to the first input of the compaof one half of the display period, and Ē

11. The analog office circuit of claim 8, in which the

rator during the consecutive frame periods.

signal generator (228) includes a

nal and has a detection sense set by a sense control signal (SENSE) that changes state halfcomparator (225) that generales the chive sig-

way furough the display period, the comparator

The eneing othe circuit of claim 8, in which:

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and sequence.

PAGE 26/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

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Yive eignal generator (128) includos:

a first Inventer (186), the first inventer having an

second inverter (174) having an input conrected to the cutput of the tirst inventer, the Second inverter having an output.

a capaditor (160) having a tinal electrodo (169) trode being connected to the input of the first the cocond electrode being connected to a and a second electrode (191), the first elecinverter and to the sample selection section, amp signal heving a duration equal to one-half

2

a recent switch (164) that discharges the capacof the display perced;

≠

seree control stone (SENSE) fruit changes tate half-way frough fre display period to take the output of one of (a) the first inventor and (b) the second inventor as the drive signal. ond inverter and operating in response to a semitching arrangement (176, 178) connected to the outputs of the first inventor and the secfor prior to the display period; and

12. The amalog drive circuit of claim 7 or 11, in which;

the drive signal generator additionally included:

roud of the inverter to the sample edection so an additional switch (203) that temporarily. coupling capacitor (201) ecupling the section, and

agnet (SCLEAR) that has a state equal to a connects the output of the first inverter to the reset switch (164) is coupled to a reference predetermined inverter breshold voltage when the input of the first inverter prior to the disptay period; and

the additional switch connects the output of the first inverter to the input of the first inverter.

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18. The analog drive closuit of daim 1, in which:

The video signal includes a color companent for each of more than one colors; and the sample selection section (329) includes: a sample alonge element (154R, 154Q, 154B) corresponding to each odor compo-152B) that opens during the sample load a cample selection gate (152R, 152Q nert, and

the analog othe circuit additionally compáses a

color component to each respective samperiod to admit the analog sample of each

ple storage eternant, and

sample output gates operating sequentially to connect the analog comple stored in each semlocated between each sample storage element and the drive signal generator (328, 428), the sampte output gale (158R, 1969, 1569) ple storage element to the drive signal genera

tiofly generates a drive signal in response to the drive signal generator (328, 428) sequenthe analog sample stored in each sample storage element.

the drive signal generator (428) includes a having opposite states in consecutive framo periods; and comparator (2.55) that generates the drive eignal, the comparator comprising a first input (A) and a second input (B) and having a detection sense set by a sense control signal (6ENSE) The analog drive chault of datm 13, in which:

a first switching element (2070, 207E) that alternately connects a mmp algual to (a) the first input and (b) the second input of ods, the ramp signed having a duration of a second switching element (2560, 256E) The comparator in consecutive frame perione-half of the frame period, and

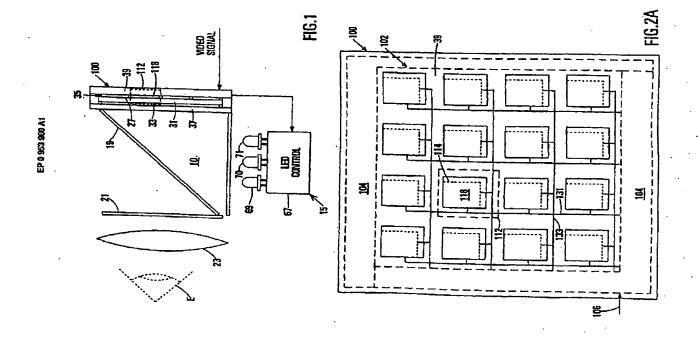
he arelog drive drout additionally comprises:

put gates to (a) the second imput of the comparator and (b) the first imput of the that attentiately connects the sample outcomparator in consecutive display periods.

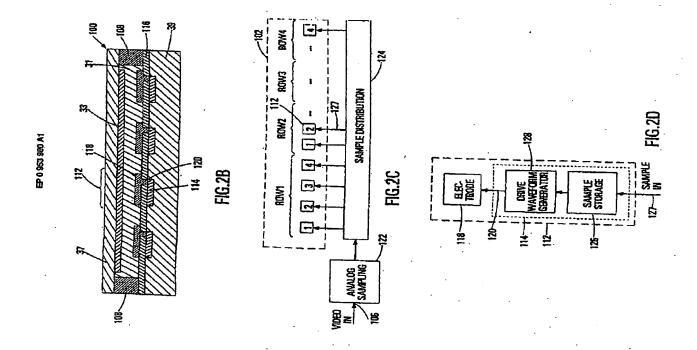
15. The enalog drive chalf of claim 1, in which:

poral portion each have a beginning; and the drive signal is composed of pulso having a raf portion eard a pulse having a second polar-ty, opposite the first polarity, of the baginaring of the second temporal portion. the first temporal portion and fre second temfirst polarity at the beginning of the first tempo16. The analog drive circuit of claim 16, in which the d'Ne signal generator includes an a.c.-coupled out-

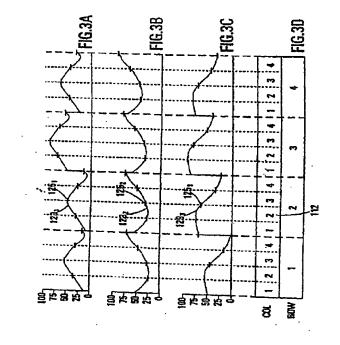
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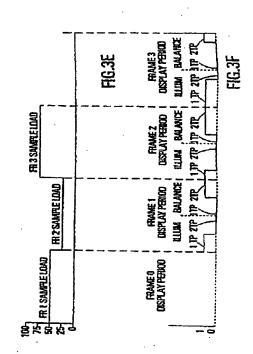


PAGE 28/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

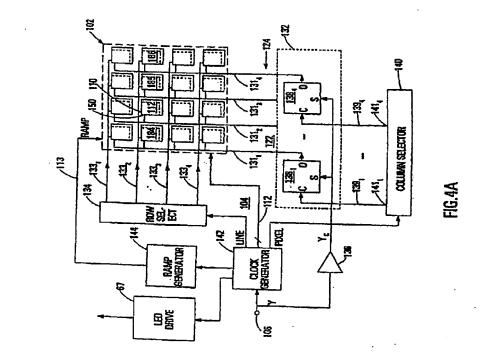


PAGE 29/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

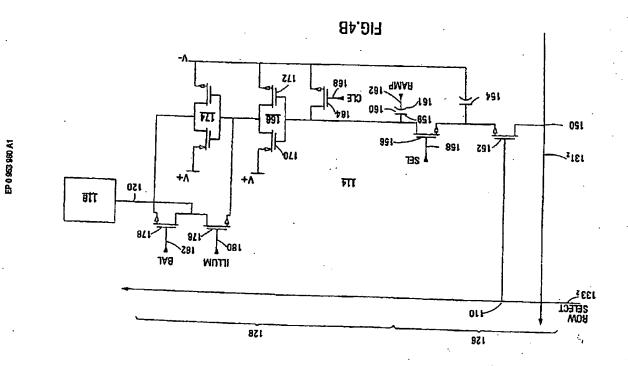




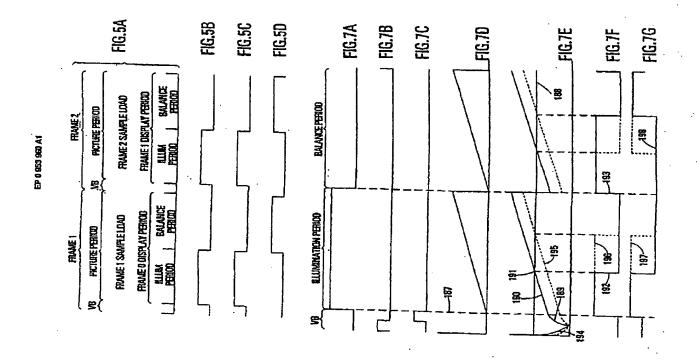
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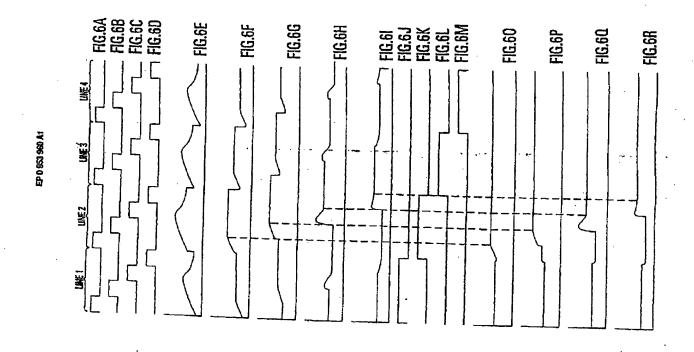


PAGE 31/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

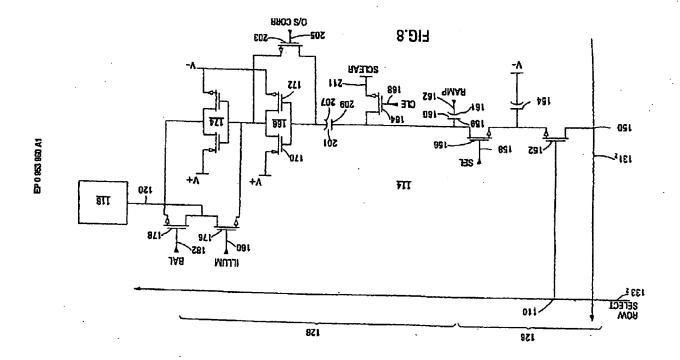


PAGE 32/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

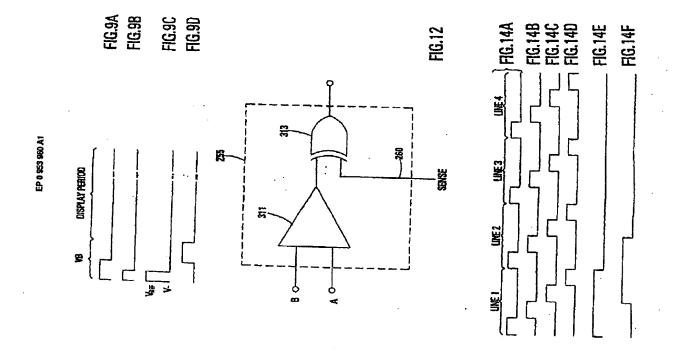


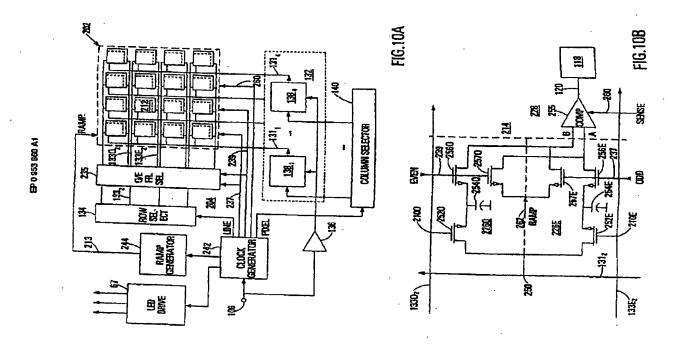


PAGE 34/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06



PAGE 35/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06





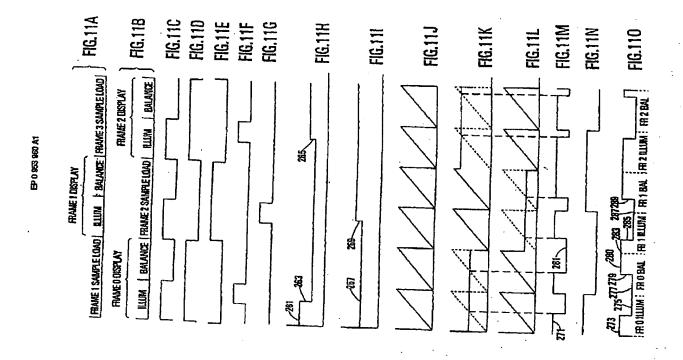
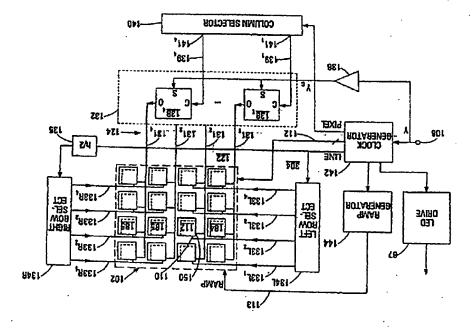
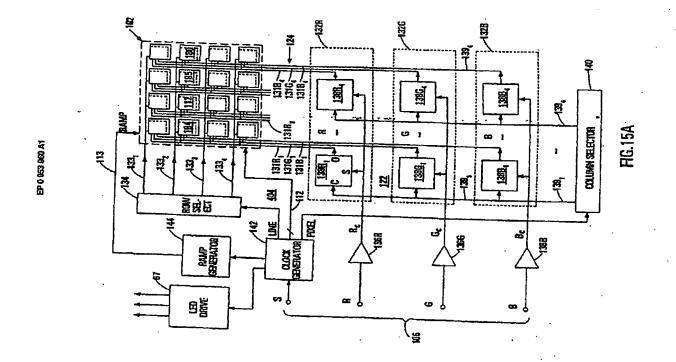
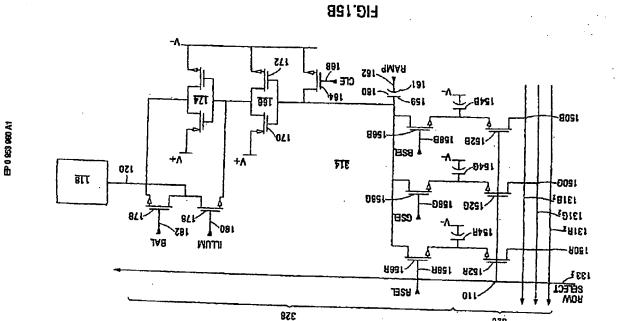


FIG.13

EP 0 953 980 A1

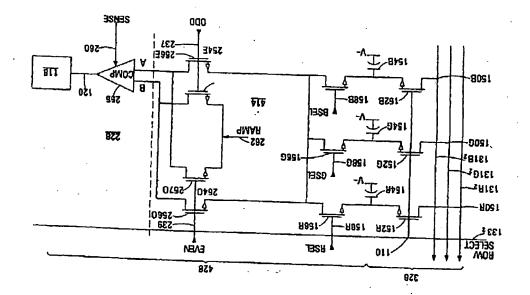




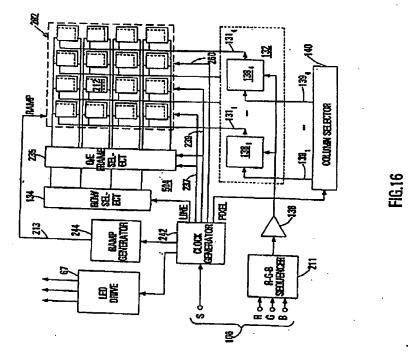


326

FIG.15C



EP 0 953 960 A1



PAGE 44/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

EP 98 12 2978 ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

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PAGE 45/79 * RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:7035185499 * DURATION (mm-ss):35-06

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